

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
112857-099

Re Application Of: Ryoichi Shimizu

Serial No.
08/883,322Filing Date
June 26, 1997Examiner
T. Tran

Group Art Unit

Invention: SELECTABLE RECORDING FRAME RATE VIDEO TAPE RECORDER

RECEIVED
JUL 09 2002
Technology Center 2600TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on
June 28, 2002

The fee for filing this Appeal Brief is: \$320.00

- ☒ A check in the amount of the fee is enclosed.
- ☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. A duplicate copy of this sheet is enclosed.
- ☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 02-1818
A duplicate copy of this sheet is enclosed.


Signature

Dated: June 28, 2002

Jeffrey H. Canfield (Reg. No. 38,404)
Bell, Boyd & Lloyd LLC
P.O. Box 1135
Chicago, IL 60690

I certify that this document and fee is being deposited
on 6/28/02 with the U.S. Postal Service as
first class mail under 37 C.F.R. 1.8 and is addressed to the
Assistant Commissioner for Patents, Washington, D.C.
20231.


Signature of Person Mailing Correspondence

Robert Buccieri

Typed or Printed Name of Person Mailing Correspondence

cc:



#22 JC
7-10-02

THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant(s): Ryoichi Shimizu
Appl. No.: 08/883,322
Filed: June 26, 1997
Title: SELECTABLE RECORDING FRAME RATE VIDEO TAPE RECORDER
Art Unit: 2615
Examiner: T. Tran
Docket No.: 112857-099

Assistant Commissioner for Patents
Washington D.C. 20231

RECEIVED
JUL 09 2002
Technology Center 2600

APPELLANT'S APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted pursuant to the Notice of Appeal submitted concurrently herewith on June 28, 2002 in the above-identified patent application.

I. REAL PARTY IN INTEREST

The real party in interest for the above-identified patent application on appeal is Sony Corporation by virtue of an Assignment executed November 19, 1997 and recorded at the United States Patent and Trademark Office at Reel 8906, Frame 0455.

II. RELATED APPEALS AND INTERFERENCES

Appellant does not believe there are any pending appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision with respect to the above-identified Appeal.

III. STATUS OF THE CLAIMS

Claims 1-14 are pending in this Application. A copy of appealed claims 1-14 is attached

in the Appendix. At present, claims 1-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,104,858 to *Suzuki* in view of U.S. Patent No. 5,229,890 to *Okauchi*. A copy of the Final Office Action mailed on December 31, 2001 and the prior art on which the rejection is based are included as Exhibit A of the Supplemental Appendix. A copy of the Advisory Action mailed on April 5, 2002 is included as Exhibit B of the Supplemental Appendix.

IV. STATUS OF THE AMENDMENTS

No amendments were filed prior to or subsequent to the Final Rejection mailed on December 31, 2001.

V. SUMMARY OF THE INVENTION

The present invention relates to a video tape recorder capable of selecting a desired frame rate when an information signal is recorded. (Specification at page 1, lines 7-8.) More specifically, the present invention relates to a video tape recorder that can simply and efficiently determine a recording mode by simultaneously recording the recording frame rate information together with different types of time code information. (Specification at page 1, lines 8-12.) Thus, the present invention is able to accurately locate a reference point indexed by either a real time code or by a frame number while operating in playback mode. (Specification at page 1, lines 12-14.)

Conventionally, video tape recorders can record time information in addition to video and audio signals. (Specification at page 1, lines 17-19.) Time information provides an index for playback and editing of the recording and it is typically coded using standard hours, minutes and seconds notation. (Specification at page 1, lines 19-21.) Thus, it is desirable to provide each video frame with a unique time code for addressing purposes. (Specification at page 1, lines 27-

28.) It is also desirable to have time codes that correspond to real time (i.e., a time code recorded for each frame), but not all standard video formats have a frame rate that allows an integer number of frames to be recorded for each second of time. (Specification at page 1, line 28 to page 2, line 4.)

For example, the National Television System Commission (NTSC) standard video signal has a frame rate of 29.97 frames per second while a high definition television (HDTV) signal has a frame rate that is precisely 30 frames per second. (Specification at page 2, lines 5-11.) Since the NTSC standard does not have an integer number of frames per second, some frames cannot be assigned a time code that corresponds to real time. (Specification at page 2, lines 12-14.) As a result, when an NTSC signal is recorded, some frames must be skipped or “dropped” to compensate for the difference, thereby resulting in a time code that is referred to as a Drop Frame stepping (DF) time code. (Specification at page 2, lines 14-22.) In contrast, signals having an integer frame rate per second such as the HDTV signal do not have to “drop” frames, thereby resulting in a time code that is referred to as a Non-Drop Frame non-stepping (NDF) time code. (Specification at page 3, lines 1-4.)

Accordingly, if no information about how to select the frame rate and the time code is provided upon reproduction (e.g., playback), then a real time process cannot be performed using the number of frames as a reference. (Specification at page 5, line 27 to page 6, line 3.) This problem is not limited to playback or reproduction of video, and can, for example, result in choppy image transition for image editing such as that used for computer animation and graphics, and the like. (Specification at page 5, lines 3-9.) Thus, Appellant recognized that to allow for reproduction in a format different from that used for recording, it would be desirable to have a video tape recorder in which the playback frame rate can be arbitrarily selected and either a NDF or a DF time code format can also be selected for playback information. (Specification at page

6, lines 17-20.)

To this end, in an embodiment of the present invention, a video tape recorder is provided which is capable of performing signal recording and reproducing processes at a plurality of different frame rates. An image signal is recorded at one selected recording frame rate, and a time code stepped in a non-drop frame as a time code at the time of its recording and a time code stepped in a drop frame are respectively recorded together with the selected recording frame rate. Thus, the playback time code information of both NDF and DF formats are simultaneously recorded in addition to the recording of recording frame rate information used in the recording mode.

VI. ISSUES

The issue on Appeal is as follows:

1. Whether claims 1-14 when taken as a whole are obvious in light of the teaching of U.S. Patent No. 6,104,858 to *Suzuki* in view of U.S. Patent No. 5,229,890 to *Okauchi*?

VII. GROUPING OF THE CLAIMS

For purposes of issue 1 presented above, claims 1-14 are considered to stand or fall together, solely for the purposes of this appeal.

VIII. ARGUMENT

Claims 1-14 of the patent application on appeal are not unpatentable under 35 U.S.C § 103(a) as being obvious in light of the teaching of U.S. Patent No. 6,104,858 to *Suzuki* in view of U.S. Patent No. 5,229,890 to *Okauchi*.

A. LEGAL STANDARDS FOR DETERMINING OBVIOUSNESS

35 U.S.C. §103(a) states that:

A patent may not be obtained.... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

In making a determination that an invention is obvious, the Patent Office has the initial burden of establishing a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S. P.Q.2d 1955, 1956 (Fed. Cir. 1993). "If the examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent." *In re Oetiker*, 24 U.S.P.Q. 2d 1443, 1444 (Fed. Cir. 1992). The Court of Appeals for the Federal Circuit has stated that the foundation facts for a *prima facie* case of obviousness are:

(1) the scope and content of the prior art; (2) the difference between the prior art and the claimed invention; and (3) the level of ordinary skill in the art...Moreover, objective indicia such as commercial success and long felt need are relevant to the determination of obviousness....Thus, each obviousness determination rests on its own facts.

In re Mayne, 41 U.S.P.Q. 2d 1451, 1453 (Fed. Cir. 1997).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference or references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *In re Fine*, 837 F.2d 1071, 5, USPQ2d 1596 (Fed. Cir. 1988). Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Finally, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ, 580 (CCPA 1974). In this respect, "[o]bviousness cannot be established by combining the teaching of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination."

ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q.2d 929, 932 (Fed. Cir. 1984).

In the present case, the Patent Office has failed to establish a prima facie case of obviousness because, even if one of ordinary skill would have been motivated to combine the references, the cited references nonetheless fail to teach or suggest every element of the claimed invention.

B. CLAIMS 1-14 ARE NOT OBVIOUS UNDER 35 U.S.C. § 103 OVER *SUZUKI* IN VIEW OF *OKAUCHI*.

Claims 1-14 are patentable over *Suzuki* and *Okauchi* because even when combined in the manner suggested by the Examiner, *Suzuki* and *Okauchi* do not teach or suggest every element of the rejected claims. Accordingly, the rejection must be reversed.

Independent claims 1, 6 and 12-14, as well dependent claims 2-5 and 7-11, stand or fall together. Each of the independent claims requires, in part, recording a plurality of time codes together with the selected recording frame rate. In this regard, claim 1 is representative. Claim 1 relates to a video tape recorder capable of performing signal recording and reproducing processes at a plurality of different frame rates. The video tape recorder includes means for recording an input image signal at a selected recording frame rate. The video tape recorder further includes means for recording a first time code stepped in a non-drop-frame format and a second time code stepped in a dropped-frame format **together** with the selected recording frame rate.

Neither *Suzuki* nor *Okauchi*, either alone or in combination, teach the features of claim 1, specifically the feature of recording a plurality of time codes simultaneously with the selected frame rate. In this regard, in the Final Office Action, the Examiner admits that *Suzuki* does not disclose means for recording a first time code stepped in a non-drop frame format and a second

time code stepped in a drop frame format on the recording medium together with the selected recording frame rate. Accordingly, the Examiner relies on the teaching of *Okauchi* to remedy the deficiencies of *Suzuki*. However, the Examiner evidently misconstrues *Okauchi*. *Okauchi*, like *Suzuki*, does not disclose means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format on the recording medium together with the selected recording frame rate.

The Examiner asserts that *Okauchi* discloses means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format on the recording medium together with the selected recording frame rate at column 5, lines 8-66.

This assertion is incorrect. In this respect, at lines 9-14, *Okauchi* clearly teaches the use of a manual switch to control a drop-frame/non-drop-frame switching signal. The drop-frame/non-drop-frame switching signal “assumes one of a H (high level) and L (low level) by selection through” the manual switch. Thus, the user can select only one of the drop frame mode and the non-drop frame mode (i.e., one format or the other based on the high or low value of the drop-frame/non-drop-frame switching signal), but not both as required by the claimed invention.

As described above, *Okauchi* discloses two different time code modes, each of which only records one type of time-code together with the selected frame rate. Nowhere does *Okauchi* disclose recording a first time code and a second time code together with the selected recording frame rate. Thus, even if one of ordinary skill in the art would have been motivated to combine the teachings of *Suzuki* and *Okauchi* as suggested by the Examiner, the result nonetheless fails to teach or suggest the claimed invention as a whole.

In the Final Office Action, the Examiner responds to Appellant’s previous arguments by reproducing column 3, lines 4-60 of *Okauchi*. The Examiner asserts that this passage of *Okauchi*

discloses that two types of frame rates are recorded along with the selected frame rate on the video tape. This assertion is incorrect. The passage cited by the Examiner merely describes how the recording system is able to identify which time code mode is selected. In this regard, the recording system formats data to be recorded and uses 8 to 10 dummy bits to identify the time code mode. When the non-drop frame mode is selected, the initial bit of the dummy bits is "0" which tells the system not to correct for time-deviation. When the drop-frame mode is selected, the dummy bits are reduced to 8 bits and the initial bit of the dummy bits is "1" which tells the system to correct for time-deviation by "dropping" certain frames. Accordingly, the dummy bits are used to identify which time code mode was selected before recording the video signal. Thus, *Okauchi* discloses that only one time code, corresponding to the selected time code mode, is recorded together with the selected frame rate on the recording medium.

In the Final Office Action, the Examiner further asserts that, for the sake of argument, even if:

Okauchi does not disclose the capability of recording both drop-frame and non-drop-frame coded pulses along with the selected recording frame rate, the user can operate the manual switch discloses (sic) in col. 5, lines 9-14 of *Okauchi* to record both drop-frame and non-drop frame coded pulses together with the selected recording frame rate.

Appellant respectfully submits that *Okauchi* does not teach or suggest that the user repeatedly switch the time code mode as suggested by the Examiner. Furthermore, even if the user were to operate the manual switch as suggested by the Examiner, only one time code would be recorded along with the selected recording frame rate, that is, only one type of time code corresponding to the selected time code mode is recorded at any given time. In contrast, the claimed invention requires that a first time code and a second time code are recorded simultaneously with the selected recording frame rate.

Moreover, if the user were to operate the switch as suggested by the Examiner, a

nonsensical result would be produced. The time code would fluctuate over the course of the recorded video signal, but the frame rate would stay the same. Thus, the video signal would not be able to be accurately reproduced. For these reasons, Appellant respectfully submits that the Examiner's suggestion is not supported by *Okauchi*, nor is it feasible to one of ordinary skill in the art, nor would it produce the claimed invention.

Finally, in the Advisory Action, the Examiner asserts that "the capability of **simultaneously** recording a plurality of time codes together with the selected frame rate is not recited in the claims." Appellant respectfully disagrees. Claim 1 clearly requires, in part, "means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format **together** with the selected recording frame rate" (emphasis added). Webster's Ninth New Collegiate Dictionary defines **together** as "at one time : SIMULTANEOUSLY" WEBSTER'S NINTH NEW COLLEGIATE DICTIONARY 1240 (9th ed. 1984). Thus, contrary to the Examiner's assertion, the capability of recording a plurality of time codes "simultaneously" with the selected frame rate is recited in the claims. As discussed above, none of the cited art teaches this feature.

In light of the preceding remarks, Appellant respectfully submits that even if one skilled in the art were to combine *Suzuki* and *Okauchi* as suggested by the Examiner, the claimed invention does not result. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness and claims 1-14 must be allowed.

IX. CONCLUSION

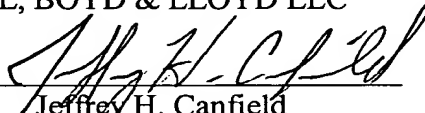
Even if one skilled in the art were to combine *Suzuki* with *Okauch*, they fail to teach or suggest every element of the claimed invention. Accordingly, the Patent Office has failed to overcome its *prima facie* burden for rejecting the claims under 35 U.S.C. §103(a). In light of the

Patent Office's failure to establish a case of *prima facie* obviousness, Appellant respectfully submits that the rejections of pending claims 1-14 as being obvious is improper in law and in fact and should therefore be reversed.

Respectfully submitted,

BELL, BOYD & LLOYD LLC

BY


Jeffrey H. Canfield
Reg. No. 38,404
P.O. Box 1135
Chicago, Illinois 60690-1135
Phone: (312) 807-4233

ATTORNEYS FOR APPELLANT

APPENDIX

1. A video tape recorder capable of performing signal recording and reproducing processes at a plurality of different frame rates, comprising:

means for recording an input image signal at a selected recording frame rate; and

means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format together with the selected recording frame rate.

2. The video tape recorder of claim 1, wherein the input image signal is recorded as a component digital image signal on a recording medium, and the time code stepped in the non-drop frame format, the time code stepped in the drop frame format, and the recording frame rate are each respectively recorded in an auxiliary area of a signal recording area on the recording medium.

3. The video tape recorder of claim 2, wherein the signal recording area of the recording medium is a video recording area.

4. The video tape recorder of claim 2, wherein the signal recording area of the recording medium is an audio recording area.

5. The video tape recorder of claim 1, wherein 59.94 Hz and 60 Hz are used as the recording frame rates.

6. A recording apparatus for recording video signals at one of a plurality of frame rates on a recording medium, comprising:

a control circuit including:

a frame rate selection circuit for selecting a frame rate from the plurality of frame rates;

a counting method selection circuit for selecting a time code counting method from a plurality of time code counting methods;

a first signal generation circuit for outputting a first controlling signal indicating the selected frame rate; and

a second signal generation circuit for outputting a second controlling signal

indicating the selected time code counting method;
a time code generator circuit for generating a plurality of time code counts, one for each of the plurality of time code counting methods;
a recording processing circuit including:
 a first recording circuit for recording the video signals on the recording medium at the selected frame rate in response to the first controlling signal from the control circuit;
 a second recording circuit for recording the plurality of time code counts from the time code generator circuit on the recording medium; and
 a third recording circuit for recording data indicating the selected frame rate on the recording medium; and
a time code method selection and recording circuit for selecting a time code count from the plurality of time code counts generated by the time code generator circuit, and for recording the selected time code count on the recording medium in response to the second controlling signal from the control circuit.

7. The recording apparatus of claim 6 wherein the plurality of frame rates include 59.94 Hz and 60 Hz.

8. The recording apparatus of claim 6 wherein the plurality of time code counting methods include a first time code counting method of the video signal using drop frame stepping and a second time code counting method of the video signal using non-drop frame stepping.

9. The recording apparatus of claim 8, wherein the video signal is recorded as a component digital image signal, and the time code count stepped in the non-drop frame method, and the recording frame rate are respectively recorded in an auxiliary area of a signal recording area of the recording medium.

10. The recording apparatus of claim 9 wherein the auxiliary area is part of a video signal recording area of the recording medium.

11. The recording apparatus of claim 9 wherein the auxiliary area is part of an

audio signal recording area of the recording medium.

12. A recording and/or reproducing apparatus for recording input audio and video signals at a one of a plurality of frame rates on a recording medium and for reproducing audio and video signals recorded on the recording medium at one of the frame rates, comprising:

control means for selecting one of the plurality of different frame rates,

for selecting a first time code counting method in which drop frame stepping is used or a second time code counting method in which non-drop frame stepping is used, and

for outputting a first control signal indicating which time code counting method is selected;

time code generating means for generating a first time code count based on the first time code counting method and a second time code count based on the second time code counting method;

recording medium processing means for recording the audio and video signal on the recording medium at the selected frame rate based on the first control signal,

for recording both the first time code count and the second time code count from the time code generating means on the recording medium,

for recording data indicating the selected frame rate on the recording medium, and

for reproducing the audio and video signal, as recorded at the selected frame rate, and the first and second time code counts from the recording medium;

time code selection means for selecting a time code counting method from among the first time code counting method and the second time code counting method based on the second control signal from the control means;

time code recording means for recording the selected time code count; and

time code reproducing means for reproducing the selected time code count recorded on the recording medium.

13. A video tape recording method for performing signal recording and reproducing processes at a plurality of frame rates, comprising the steps of:

separating a plurality of types of time code information and recording frame rate information according to a reproduced signal; and

selecting a playback frame rate for the reproduced signal and a time code for the selected frame rate when reproduced image information is accessed via real-time units and frame number units.

14. A method of recording video signals at one of a plurality of frame rates on a recording medium, comprising the steps of:

- selecting a frame rate from the plurality of frame rates;
- selecting a time code counting method from a plurality of time code counting methods;
- outputting a first controlling signal indicating the selected frame rate;
- outputting a second controlling signal indicating the selected time code counting method;
- generating a plurality of time code counts, one for each of the plurality of time code counting methods;
- recording the video signals on the recording medium at the selected frame rate in response to the first controlling signal;
- recording the plurality of time code counts on the recording medium;
- recording data indicating the selected frame rate on the recording medium;
- selecting a time code count from the plurality of time code counts; and
- recording the selected time code count on the recording medium in response to the second controlling signal.

SUPPLEMENTAL APPENDIX

EXHIBIT A

FINAL OFFICE ACTION AND REFERENCES

RECEIVED

JUL 09 2002

Office Action Summary

JUL 05 2002

Application No.
08/883,322

Applicant(s)

Technology Center 2600

Examiner

Thai Tran

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Oct 19, 2001
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

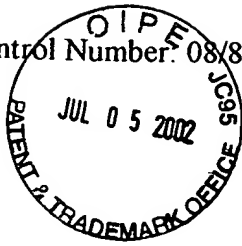
- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

Application/Control Number: 08/883,322

Art Unit: 2615



RECEIVED
JUL 09 2002
Technology Center 2600

Page 2

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki ('858) in view of Okauchi ('890) as set forth in paragraph #3 of the last Office Action.

Regarding claim 1, Suzuki discloses an a video tape recorder (Fig. 5 and Fig. 17) capable of performing signal recording and reproducing process at a plurality of different frame rates having means (column 7, lines 9-42 and column 17, lines 6-9) for recording an input image signal at a selected recording frame rate. However, Suzuki does not specifically discloses means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format together with the selected recording frame rate.

Art Unit: 2615

Okauchi teaches a data recording system for use in a video tape recorder having means (column 5, lines 8-66) for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format together with the selected recording frame rate so that the time code in recording is coincidence with the real time according to the CTL coding system.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the time code recorder as taught by Okauchi into Suzuki's system in order to coincide the real time and the time code in recording according to the CTL coding system.

Regarding claim 2, the combination of Suzuki and Okauchi teaches that the input image signal is recorded as a component digital image signal on a recording medium (column 11, lines 4-57 of Suzuki), and the time code stepped in the non-drop frame format, the time code stepped in the drop frame format, and the recording frame rate are each respectively recorded in an auxiliary area of the signal recording area on the recording medium (column 5, lines 8-66 of Okauchi and column 11, lines 40-48 of Suzuki).

Regarding claim 3, Suzuki discloses that the signal recording area of the recording medium is a video recording area (column 14, lines 30-45).

Regarding claim 4, Suzuki discloses that the signal recording area of the recording medium is a audio recording area (column 14, lines 30-45).

Art Unit: 2615

Regarding claim 5, the claimed 59.94 Hz is met by the NTSC signal disclosed in column 7, lines 30-42) and the claimed 60 Hz is met by the MUSE signal disclosed in column 7, lines 9-16 and column 17, lines 6-9 of Suzuki.

Regarding claim 6, the claimed a frame rate selection circuit for selecting a frame rate from the plurality of frame rates is met by the switch 8 of Suzuki (column 8, line 64 to column 9, line 31 of Suzuki); the claimed a counting method selection circuit for selecting a time code counting method from a plurality of time code counting methods is met by column 5, lines 8-62 of Okauchi; the claimed a first signal generation circuit for outputting a first control signal indicating the selected frame rate is met by switch 8 of Suzuki (column 8, line 64 to column 9, line 31 of Suzuki); the claimed a second signal generation circuit for outputting a second controlling signal indicating the selected time code is met by column 5, lines 8-62 of Okauchi; the claimed a time code generator circuit for generating a plurality of time code counts, one for each of the plurality of time code counting methods is met by column 5, lines 8-62 of Okauchi; the claimed a first recording circuit for recording the video signals on the recording medium at the selected frame rate in response to the first controlling signal from the control circuit is met by magnetic heads 1A, 1B, 2A and 2B of Fig. 5 of Suzuki; the claimed a second recording circuit for recording the plurality of time code counts from the time code generator circuit on the recording medium is met by the magnetic head 8 of Fig. 2 of Okauchi; the claimed a third recording circuit for recording data indicating the selected frame rate on the recording medium is met by column 11, lines 40-48 of Suzuki; and wherein a time code method selection and recording circuit for selecting a time

Art Unit: 2615

code count from the plurality of time code counts generated by the time code generator circuit, and for recording the selected time code count on the recording medium in response to the second controlling signal from the control circuit is met by column 5, lines 8-66 of Okauchi.

Claim 7 is rejected for the same reasons as discussed in claim 5 above.

Regarding claim 8, the claimed wherein the plurality of time code counting methods include a first time code counting method of the video signal using drop frame stepping and a second time code counting method of the video signal using non-drop frame stepping is met by column 5, lines 8-66 of Okauchi.

Claim 9 is rejected for the same reasons as discussed in claim 2 above.

Claim 10 is rejected for the same reasons as discussed in claim 3 above.

Claim 11 is rejected for the same reasons as discussed in claim 4 above.

Claim 12 is rejected for the same reasons as discussed in claims 1 and 6 above and the additional claimed recording medium processing means for recording the audio and video signal on the recording medium as the selected frame rate based on the first control signal is met by column 14, lines 30-45 of Suzuki and the claimed time code reproducing means for reproducing the selected time code count recorded on the recording medium is met by column 5, line 64 to column 6, line 11 of Okauchi.

Regarding claim 13, Suzuki discloses a video tape recording method for performing signal recording and reproducing processes at a plurality of frame rates (Fig. 5 and Fig. 17) having the steps of separating the time code information and recording frame rate information according to a

Art Unit: 2615

reproduced signal (TCI discriminators 50 and 51 of Fig. 17 and column 24, lines 30-55) and selecting a playback frame rate for the reproduced signal and a time code for the selected frame rate (column 18, lines 63-67 and column 24, lines 30-55). However, Suzuki does not specifically disclose a plurality of types of time code information and the claimed reproduced image information is accessed via real-time units and frame number units.

Okauchi teaches a data recording/reproducing system for use in a video tape recorder having means (column 5, lines 8-66 and column 5, line 63 to column 6, line 21) for recording/reproducing a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format together with the selected recording frame rate so that the time code in recording is coincidence with the real time according to the CTL coding system and that the video signal is reproduced via real-time units and frame number units (column 1, lines 6-52).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the time code recorder/reproducer as taught by Okauchi into Suzuki's system in order to coincide the real time and the time code in recording according to the CTL coding system.

The method claim 14 is rejected for the same reasons as discussed in apparatus claims 1 and 6 above.

Response to Arguments

Art Unit: 2615

4. Applicant's arguments filed Oct. 19, 2001 have been fully considered but they are not persuasive.

In re pages 1-3, applicant argues that Susuki or Okauchi does not teach or suggest the claimed "means for recording a first time code stepped in a non-drop-frame format and a second time code stepped in a dropped-frame format together with the selected recording frame rate" as recited in claim 1; "a second recording circuit for recording the plurality of time code counts from the time code generator circuit on the recording medium" and "a time code method selection and recording circuit for selecting a time code count from the plurality of time code counts generated by the time code generator circuit, and for recording the selected time code count on the recording medium in response to the second controlling signal from the control circuit" as recited in claim 6; "means for recording both the first time code count and the second time code count from the time code generating means on the recording medium" as well as "a time code selection means for selecting a time code counting method from among the first time code counting method and the second time code counting method based on the second control signal from the control means" as recited in claim 12; and "recording the plurality of time code counts on the recording medium" as recited in claim 14 because Okauchi only records only type of time-code pulses on the tape: either drop-frame coded pulses or non-drop frame coded pulses and nowhere does Okauchi et al disclose recording both drop-frame and non-drop frame pulses on the tape.

In response, the examiner respectfully disagrees. Okauchi discloses in col. 3, lines 4-60 that "A data recording system for use in VTRs according to a first embodiment ... **In the case of**

Art Unit: 2615

NTSC, since the accurate frame number is 29.97 frame per second, the frame number due to counting the CTL pulses deviates with respect to the real time. This deviation results in 108 frames (3.6 seconds) per hour and hence provides an important problem if working for a long time. The correction of this deviation can be effected with 108 bits being reduced from the number of the dummy bits per hour ($10 \text{ bits} \times 60 \times 60 / 2 = 18000$). More specifically, the number of the dummy bits in the time code having the data representing every minute on the minute (00 second) except for every 10 minutes (e.e., 0, 10, 20, 30, 40 and 50 minutes) is reduced by 2 bits so as to become 8 bits, that is, $(60-2) \times 2 \text{ bits} = 108 \text{ bits}$...Of these 8 or 10 dummy bits, the initial bit is for distinguishing between a correction mode or a non-correction mode. When the initial bit is "0", the non-correction mode (non-drop frame mode) is taken so as not to perform the time deviation correction. When the initial bit is "1", the correction mode (drop frame mode) is performed so that the number of the dummy bits is determined to be 8 (including the initial bit) at every minute on the 20 minute (00 second) except for every 10 minutes (0, 10, 20, 30, 40 and 50 minutes)..." From the above passage, it is clear that, for the selected frame rate (NTSC, 29.97 frame per second), two types of time codes (non-drop frame mode, 10 dummy bits, and drop frame mode, 8 dummy bits) are recorded along with the selected frame rate on the video tape.

Even if, arguendo, that col. 3, lines 4-60 of Okauchi does not disclose the capability of recording both drop-frame and non-drop-frame coded pulses along with the selected recording frame rate, the user can operate the manual switch disclosed in col. 5, lines 9-14 of Okauchi to

Art Unit: 2615

record both drop-frame and non-drop frame coded pulses together with the selected recording frame rate.

Since Okauchi discloses the claimed capability of recording both drop-frame and non-drop frame coded pulses together with the selected recording frame rate on the video tape, the claimed “means for recording a first time code stepped in a non-drop-frame format and a second time code stepped in a dropped-frame format together with the selected recording frame rate” as recited in claim 1; “a second recording circuit for recording the plurality of time code counts from the time code generator circuit on the recording medium” and “a time code method selection and recording circuit for selecting a time code count from the plurality of time code counts generated by the time code generator circuit, and for recording the selected time code count on the recording medium in response to the second controlling signal from the control circuit” as recited in claim 6; “means for recording both the first time code count and the second time code count from the time code generating means on the recording medium” as well as “a time code selection means for selecting a time code counting method from among the first time code counting method and the second time code counting method based on the second control signal from the control means” as recited in claim 12; and “recording the plurality of time code counts on the recording medium” as recited in claim 14 are taught or suggested in col. 5, lines 8-66 of Okauchi.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2615

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

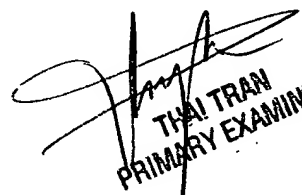
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Tran whose telephone number is (703) 305-4725. The examiner can normally be reached on Mon. To Friday, 8:00AM to 5:30 PM.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TTQ

December 30, 2001


THAI TRAN
PRIMARY EXAMINER



US005229890A

United States Patent [19]

Okauchi

[11] Patent Number: 5,229,890

[45] Date of Patent: Jul. 20, 1993

[54] DATA RECORDING SYSTEM FOR USE IN VIDEO TAPE RECORDER

[75] Inventor: Takeshi Okauchi, Chigasaki, Japan

[73] Assignee: Victor Company of Japan, Ltd., Japan

[21] Appl. No.: 548,336

[22] Filed: Jul. 5, 1990

[30] Foreign Application Priority Data

Jul. 7, 1989 [JP] Japan 1-176493

Jul. 7, 1989 [JP] Japan 1-176494

[51] Int. Cl.⁵ G11B 27/02

[52] U.S. Cl. 360/14.2; 360/14.3

[58] Field of Search 360/14.1, 14.2, 14.3, 360/33.1

[56] References Cited

U.S. PATENT DOCUMENTS

3,681,524 8/1972 Nicholls 360/14.3 X

5,018,027 5/1991 Roggendorf 360/14.2

FOREIGN PATENT DOCUMENTS

57-34633 7/1982 Japan .

OTHER PUBLICATIONS

Nishimoto, Naomichi; Okauchi, Takeshi; Kitazawa, Hiroaki: VHS VCR With Index and Address Search

System; In: IEEE Transactions on Consumer Electronics, vol. CE-33, No. 3, Aug. 1987, pp. 220 to 224.

Primary Examiner—Andrew L. Sniezek

Attorney, Agent, or Firm—Lowe, Price, LeBlanc & Becker

[57] ABSTRACT

A data recording system for use in video tape recorders selects one of a plurality of data including position information of a magnetic tape on and from which a video signal is recorded and reproduced by the video tape recorder, and controls the duty cycle of control pulses in accordance with the selected data when recording the control pulses in a control track of the magnetic tape. The data recording system is arranged to add dummy bits to a data block including the control pulses and to change the number of the dummy bits at a predetermined period. The dummy bits are added at the tailing end of the data block following the time code, and the first bit of the dummy bits represents the number of the dummy bits and is disposed in a predetermined position related to the leading bit of the data block. This arrangement corrects the time deviation of the time codes without skipping the contents of the time code data.

9 Claims, 5 Drawing Sheets

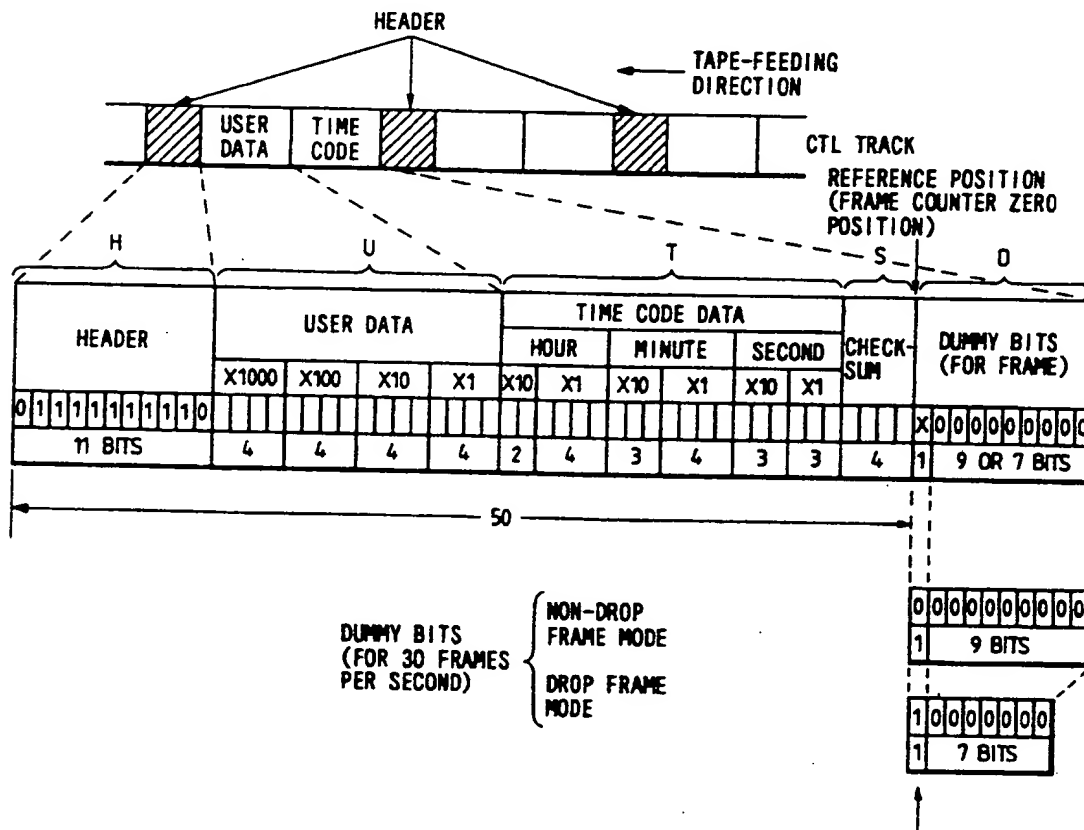


FIG. 1

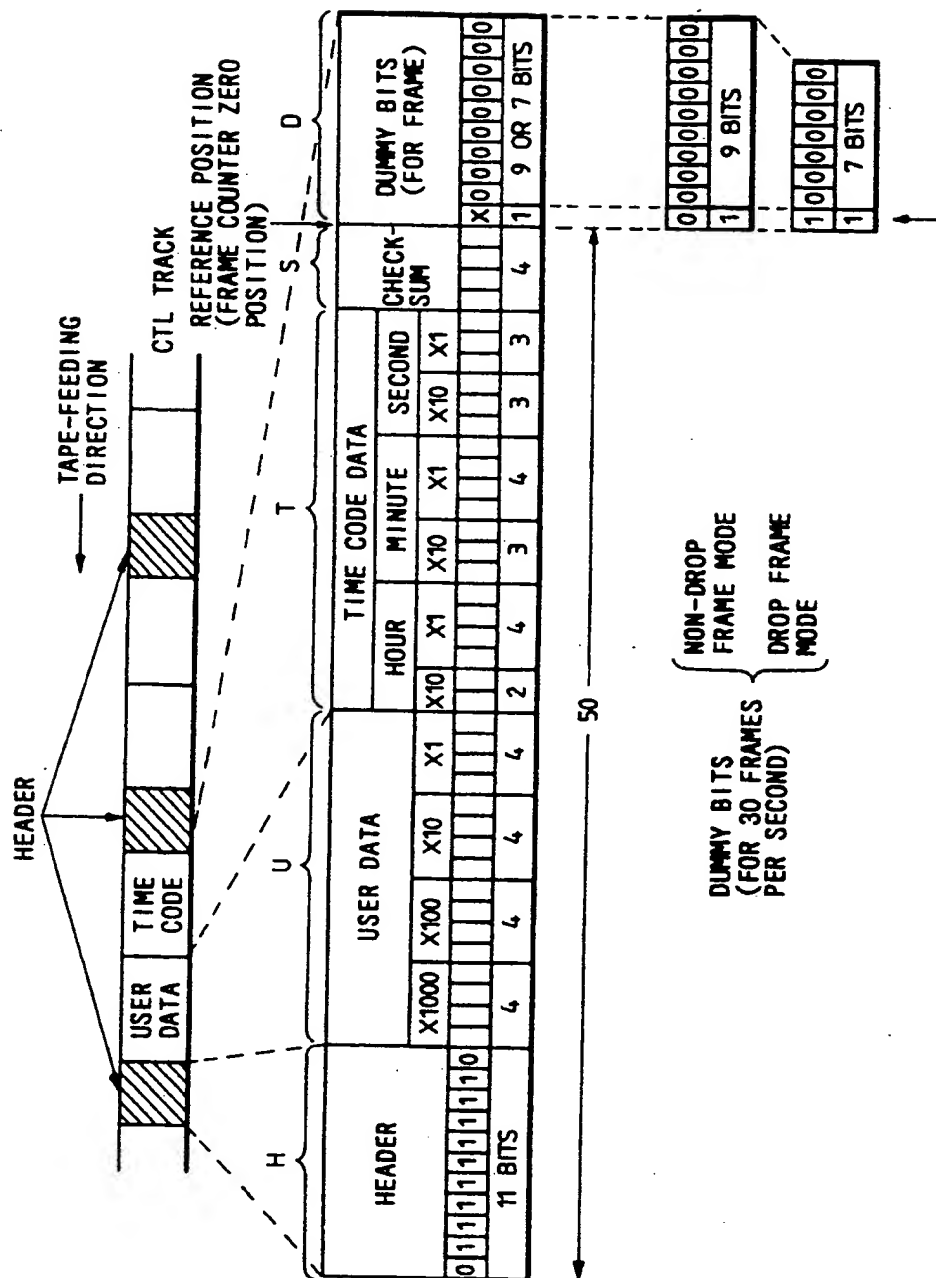


FIG. 2

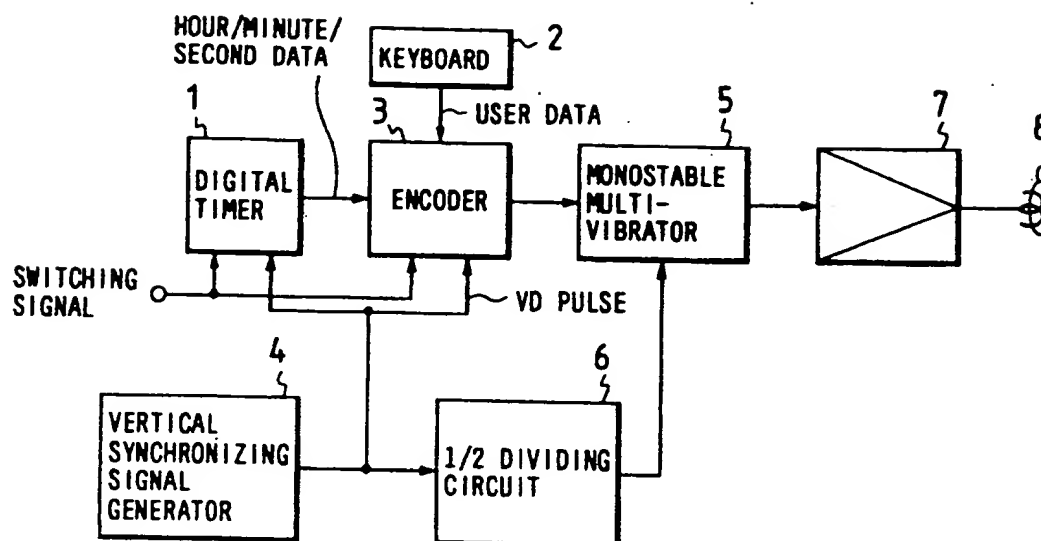


FIG. 4

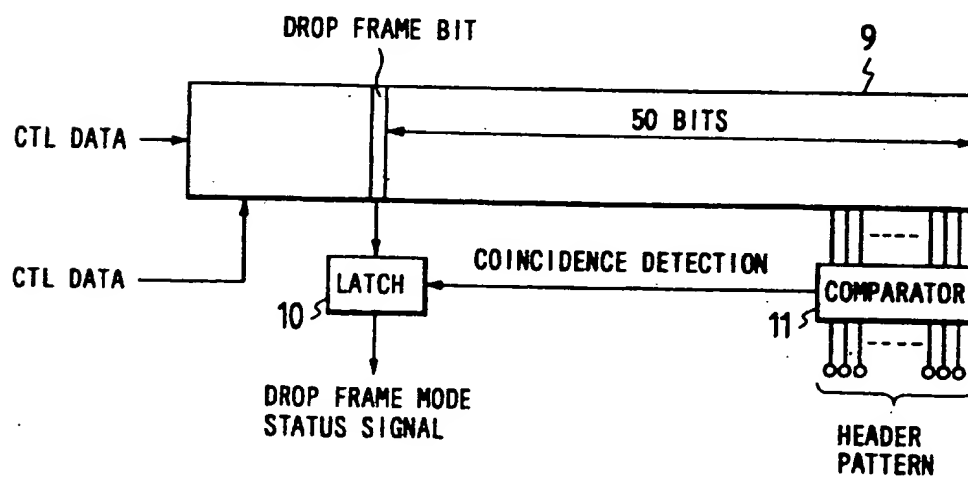


FIG. 3

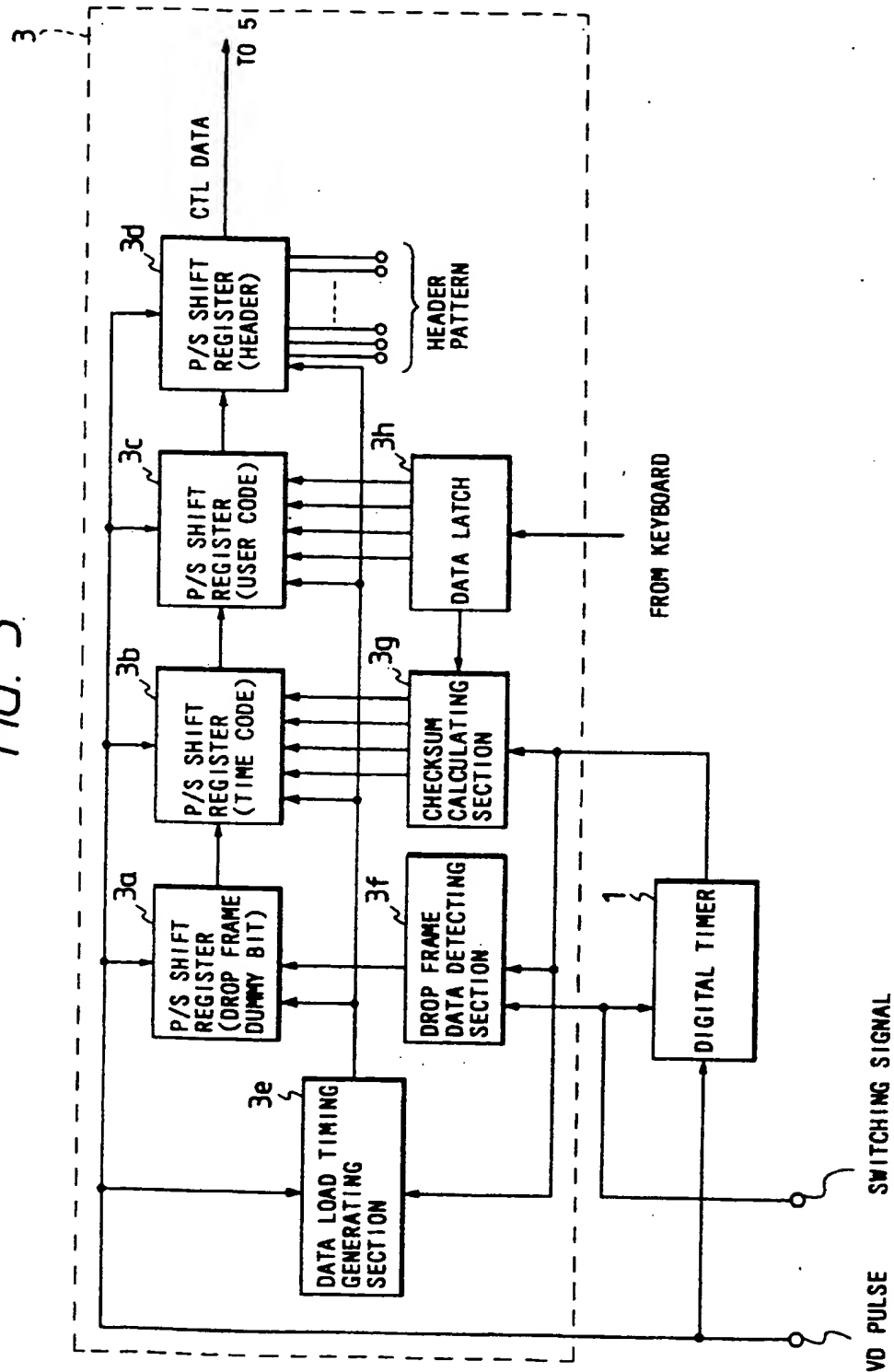


FIG. 5

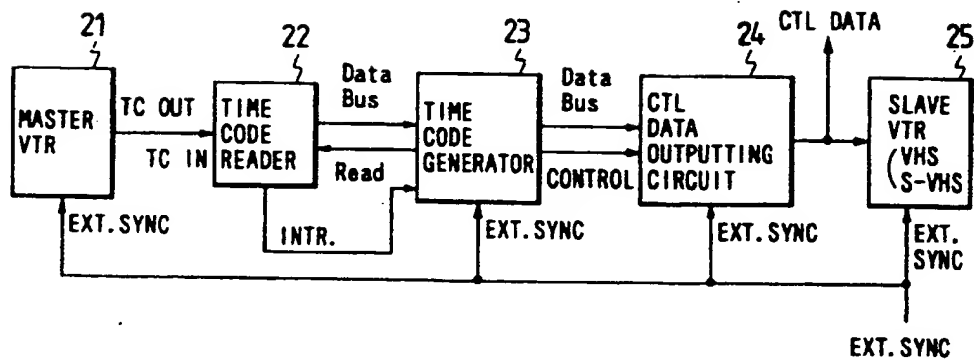


FIG. 6

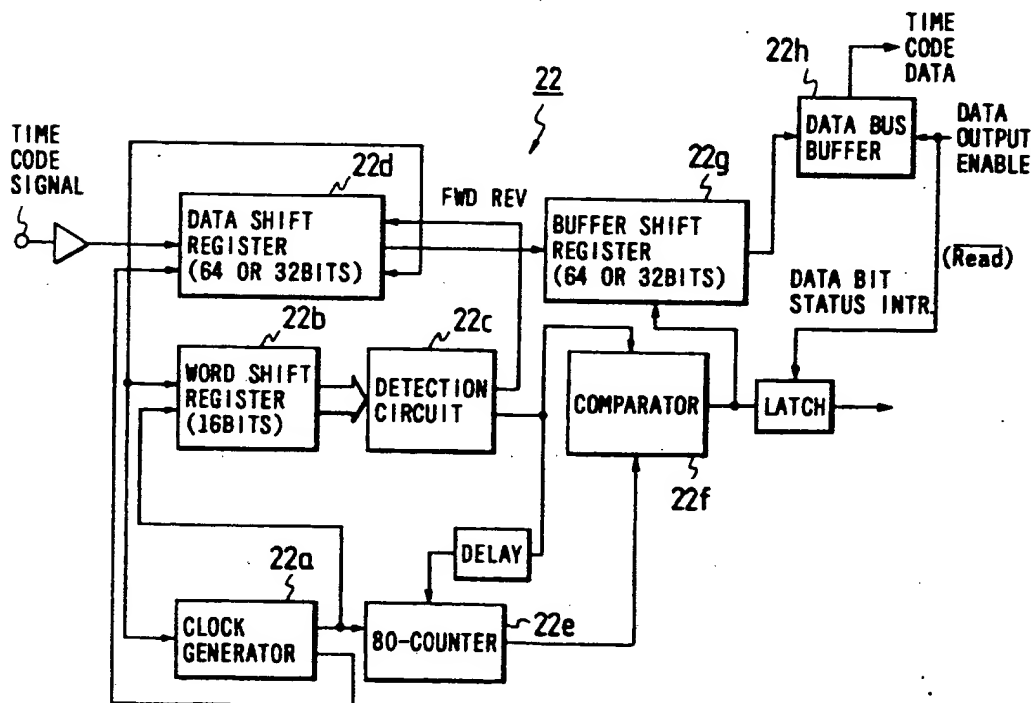


FIG. 7

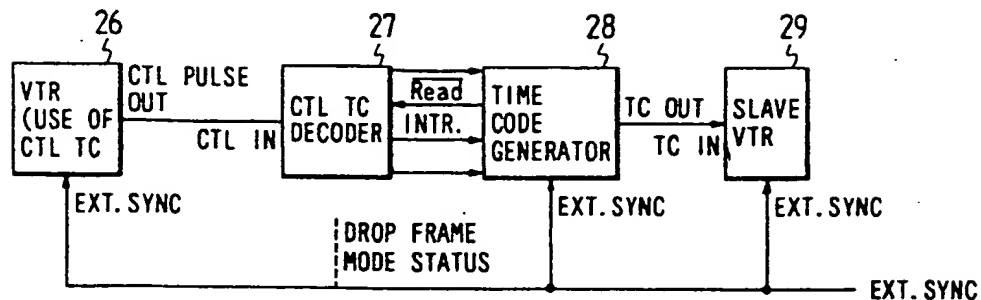


FIG. 8

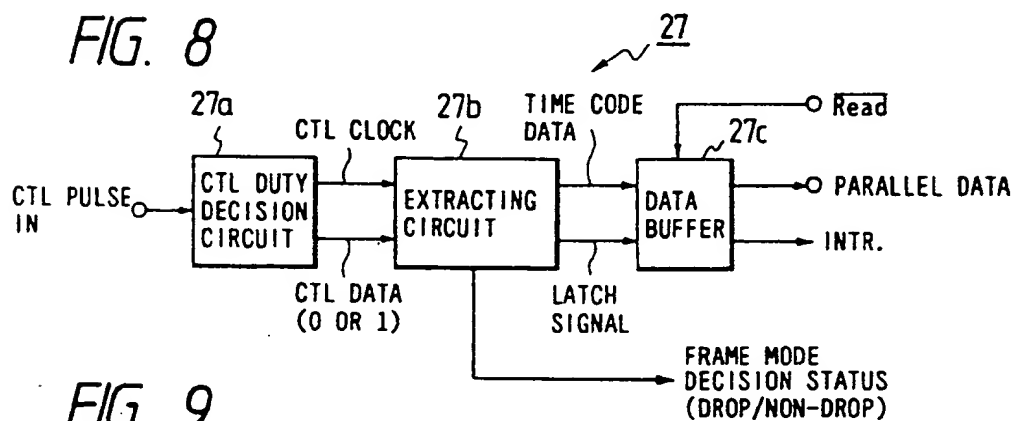
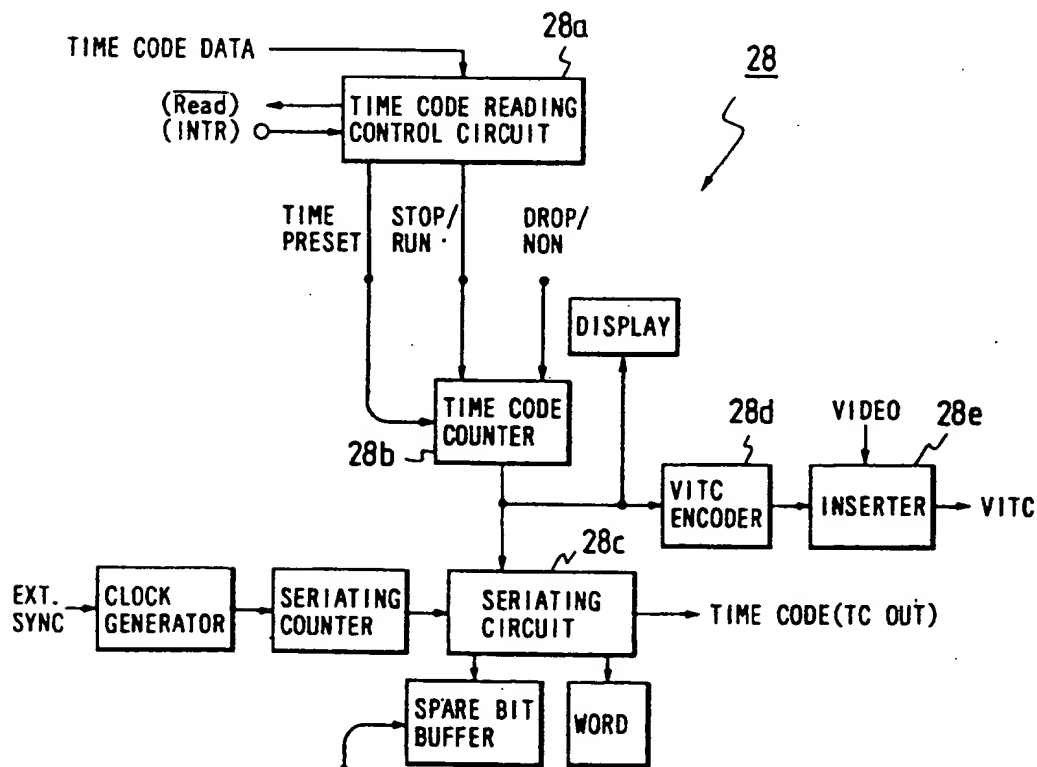


FIG. 9



DATA RECORDING SYSTEM FOR USE IN VIDEO TAPE RECORDER

BACKGROUND OF THE INVENTION

The present invention relates generally to a data recording system for recording data relating to position information and specific functions in a control track of a magnetic tape, and is applicable particularly, but not exclusively, to video tape recorders (which will hereinafter be referred to as VTRs).

In conventional VTRs, a data recording/reproducing system based upon the so-called CTL coding system, in which data relating to tape-position information and comment information are recorded in a control track with the duty cycle modulation (e.g., PWM) of control pulses (CTL pulses), is employed for enabling users to access a desired position randomly. Since various types of data are selectively recorded on a control track and reproduced therefrom, such a data recording system can be lower-priced in construction as compared with the SMPTE time code recording/reproducing system which records the absolute position of a magnetic tape with respect to the recording start position with the absolute position being expressed in a pulse form and, in addition, allows freely recording various information with an extremely simple operation.

Since it is general that the period of the control pulses is one frame period (1/30 sec. period in NTSC systems), in the method of recording data with the duty cycle of the control pulses being arranged to be variable, the data transmission bit rate is extremely small to be 30 bits per second and, in the case of recording a code such as a time code which is constructed as a data block with a great number of bits, the recording/reproduction of one data block consumes several seconds. When recording the time code by means of the CTL coding system, since the CTL coding system records only one bit per frame, it is impossible to directly record the code format in the same manner as the SMPTE time code which is constructed with 80 bits per frame. Thus, the address code is treated as the time data and recorded on a tape at a predetermined time interval (for example, every minute) so that the frame counter is reset at the address code and counts the CTL pulses for indicating a playing time. There is a problem which arises with such a CTL coding system, however, in that the timing of resetting is shifted if even one of the data in the address code is lost. In addition, in the case of an NTSC color signal, because a nominal frame number is 29.97 frames per second, the time code substantially becomes difficult to be coincident with the real time.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a data recording system for use in VTRs which is capable of coincidence with the real time in recording the time code according to the CTL coding system.

One feature of a VTR data recording system according to the present invention is that, for recording a time code in accordance with the CTL coding system, dummy bits are added to a data block and the number of the dummy bits is changed at a predetermined period. That is, according to the present invention, a VTR data recording system is provided which selects one of a plurality of data including position information of a magnetic tape on and from which a video signal is recorded and reproduced by means of a VTR and, in

accordance with the selected data controls the duty cycle of control pulses produced with a predetermined-period when recording the control pulses in a control track of the magnetic tape. The data recording system comprises means for adding dummy bits to a data block comprising the control pulses representing the time code data and further means for periodically changing the number of the dummy bits.

Another feature of the VTR data recording system according to this invention is that, for recording a time code in accordance with the CTL coding system, dummy bits are added to a rear portion of a data block and the number of the dummy bits is changed at a predetermined period when recording the data block in a control track of a magnetic tape, and further a bit which is in a predetermined position relation to the head bit of the data block is used as a decision bit representing the number of the dummy bits. That is, according to the present invention, a VTR data recording system is provided which selects one of a plurality of data, including position information of a magnetic tape on and from which a video signal is recorded and reproduced by means of a VTR, and which controls the duty cycle of predetermined-period-produced control pulses in accordance with the selected data when recording the control pulses in a control track of the magnetic tape. The data recording system comprises means for adding dummy bits to a rear portion of a data block including the control pulses representing the time code data, means for changing the number of the dummy bits at a predetermined period, and means for setting as a decision bit representing the number of the dummy bits a bit which is in a predetermined position relation to the head bit of the data block.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and features of the present invention will become more readily apparent from the following detailed description of the preferred embodiments taken in conjunction with the accompanying drawings in which:

FIG. 1 is an illustration of a signal format of data to be recorded by a data recording system of this invention;

FIG. 2 is a block diagram showing an arrangement of a data recording system according to a first embodiment of this invention;

FIG. 3 is block diagram showing an arrangement of an encoder of the FIG. 2 data recording system;

FIG. 4 is an illustration of a decoder employed for the data recorded by the FIG. 2 data recording system;

FIG. 5 is a block diagram showing an arrangement of a data recording system according to a second embodiment of the present invention;

FIG. 6 is a block diagram showing an arrangement of a SMPTE time code reader of the FIG. 5 data recording system;

FIG. 7 is a block diagram showing an arrangement of a data recording system according to a third embodiment of this invention;

FIG. 8 is a block diagram showing an arrangement of a CTL time code decoder of the FIG. 7 data recording system; and

FIG. 9 is a block diagram showing a time code generator of the FIG. 7 data recording system.

DETAILED DESCRIPTION OF THE INVENTION

A data recording system for use in VTRs according to a first embodiment of the present invention will be described hereinbelow. The data recording system is arranged such that, in order to correct the time deviation of the time code in the CTL coding system, dummy bits are provided in a code frame so that the number of the dummy bits is changed at a predetermined period. That is, in recording the time code in accordance with the CTL coding system, in the case of NTSC, dummy bits (10 bits) are added to a 50-bit code block in order to achieve the time coincidence with the real time. In the case of NTSC, since the accurate frame number is 29.97 frame per second, the frame number due to counting the CTL pulses deviates with respect to the real time. This deviation results in 108 frames (3.6 seconds) per hour and hence provides an important problem if working for a long time. The correction of this deviation can be effected with 108 bits being reduced from the number of the dummy bits per hour ($10 \text{ bits} \times 60 \times 60 / 2 = 18000$). More specifically, the number of the dummy bits in the time code having the data representing every minute on the minute (00 second) except for every 10 minutes (i.e., 0, 10, 20, 30, 40 and 50 minutes) is reduced by 2 bits so as to become 8 bits, that is, $(60 - 6) \times 2 \text{ bits} = 108 \text{ bits}$.

FIG. 1 shows a format of data to be recorded by the data recording system according to this embodiment. In FIG. 1, character H represents a header comprising 11 fixed bits and character U designates 16 user bits (4 bit BCD 4 figures) for recording the program numbers or others through an input device such as keyboard by the users. Further, character T denotes 19-bit (BCD 6 figures) time information data for expressing the present time in units of hour, minute and second. The initial 2 bits are for showing the 10-place of "hour", the next 4 bits are for showing the 1-place of "hour", the following 3 bits are for showing the 10-place of "minute", the next 4 bits are for showing the 1-place of "minute", the next 3 bits show the 10-place of "second" and the following 3 bits show the 1-place of "second". Further, character S depicts a 4-bit checksum. Still further, character D represents 8 or 10 dummy bits. Of these 8 or 10 dummy bits, the initial bit is for distinguishing between a correction mode and a non-correction mode. When the initial bit is "0", the non-correction mode (non-drop frame mode) is taken so as not to perform the time-deviation correction. When the initial bit is "1", the correction mode (drop frame mode) is performed so that the number of the dummy bits is determined to be 8 (including the initial bit) at every minute on the 20 minute (00 second) except for every 10 minutes (0, 10, 20, 30, 40 and 50 minutes). Here, since one data frame comprising 60 bits corresponds to about 2 seconds in the case of the NTSC 29.97-frame-per-second video signal (for example), the 1-place of "second" in the time information data T may show only 5 values, i.e., 0, 2, 4, 6, and 8 seconds, and hence only 3 bits can be used therefor.

According to the above-mentioned signal format to be recorded by the data recording system of this embodiment, without skipping the time code data, the time deviation correction can be performed with change of the data length in the data block. In addition, the data in the time code data can directly be used for the 25-frame-per-second video signal in the PAL, SECAM or the like without generation of the time deviation.

As described above, the dummy bits are added to a data block for the purposes of controlling the real time in recording the time code in accordance with the CTL coding system, and the number of the dummy bits is reduced to be 8 in the drop frame mode and the number of the dummy bits is maintained to be 10 in the non-drop frame mode. Here, the drop frame mode is required if operation such as an edit is performed in correspondence with the real time, while the non-drop frame mode is advantageously taken in home-use VTRs in which the operation performed in correspondence with the real time is not required, because the process for the non-drop frame is simple. Accordingly, it is better to properly use both the modes. However, it is impossible to discriminate between both the modes by the code itself. Thus, the first bit of the dummy bits is used as a decision bit for distinguishing between the drop frame mode and the non-drop frame mode. That is, as illustrated in FIG. 1, in recording the code, the decision bit is arranged to assume "1" in the case of the drop frame mode and take "0" in the case of the non-drop frame mode.

Moreover, the dummy bits are recorded at the rear side of the time data block as illustrated in FIG. 1. This is for always fixing the decision bit to the 51st bit from the leading bit of the time code, thereby immediately distinguishing between the drop frame mode and the non-drop frame mode in reading out the code. If the dummy bits are placed at the front side of the data block, the position of the decision bit varies in accordance with the number of the dummy bits so that difficulty is encountered to immediately performing the mode decision. More specifically, when decoding the time code in reproduction, the decision between the drop frame mode and the non-drop frame mode is made in accordance with the first bit of the dummy bits. Since the dummy bits are placed at the rear side of the data block, the decision of the mode for the time code data in the data block can immediately be made by checking the contents of the 51st bit from the leading bit of the header, and since the dummy bits whose bit length varies at a predetermined period are placed at the last portion of the data block, the decision can be made even if reading the user data and the time code data.

If the dummy bits are provided between the header and the user bits, the positions of the respective data are shifted by 2 bits with respect to the header in accordance with the number (8 or 10) of the dummy bits. Further, if the dummy bits are provided at the front side of the header, the decision bit which is the 51st bit from the leading bit of the header becomes difficult to be used for the next data block. Still further, in the case of checking the decision bit of the dummy bit before the header detection by using an appropriate memory, the position of the decision bit varies in accordance with the number of the dummy bits, and therefore it becomes impossible to immediately perform the mode decision.

FIG. 2 is a block diagram showing the data recording system of this embodiment which records the FIG. 1 code format in a CTL track of a magnetic tape. In FIG. 2, illustrated at numeral 1 is a known digital timer which outputs hour/minute/second data. The digital output of the digital timer 1 is supplied to an encoder 3 which is also responsive to a signal (user data) from a keyboard 2 so as to output coded pulses. The coded pulses are arranged to be synchronous with clocks (VD pulses) from a vertical synchronizing signal generating circuit 4 so as to prevent variation of the time-axis. The output

5

signal of the encoder 3 is applied to a monostable multivibrator 5 so as to modulate a period obtained by dividing the clock frequency into $\frac{1}{4}$ in a frequency divider 6, thereby obtaining time-coded pulses. Thereafter, the time-coded pulses are supplied to a recording amplifier 7 and then fed to a well known CTL head 8 to be recorded as the control track of the magnetic tape.

FIG. 3 is a block diagram showing an arrangement of the encoder 3 illustrated in FIG. 2. In FIG. 3, a drop-frame/non-drop frame switching signal supplied to both the digital timer 1 and encoder 3 is a signal which assumes one of H (high level) and L (low level) by selection through a manual switch, not shown, and is similar to the signal used for the SMPTE. The digital timer 1 is a hour/minute/second frame counter and receives a VD pulse as a clock. The count value thereof is controlled as time data (hour/minute/second frame) and supplied as parallel data to the encoder 3. In the case that the drop frame mode is selected in accordance with the drop frame/non-drop frame switching signal, it is in advance reset so as to skip the count value. The skipping is made for 2 frames, i.e., 0 and 1, at every minute on the minute (00 second) other than every 10 minutes (0, 10, 20, 30, 40 and 50 minutes). For this digital timer 1, it is possible to use a time code generator IC (for example, EEC0-5200 manufactured by Sony Co., Ltd). The encoder 3 is equipped with parallel-serial (P/S) shift registers 3a to 3d, a data load timing generating section 3e, a drop frame data detecting section 3f, a checksum calculating section 3g and a data latch 3h. The respective P/S shift registers 3a to 3d are for the drop frame and dummy bits, the time code, the user code, and the header. The data load timing generating section 3e controls the writing timing of data into the respective P/S shift registers 3a to 3d and is responsive to the output signal of the digital timer 1 and the VD pulse. The output of the digital timer 1 is supplied to the drop frame data detecting section 3f and further to the checksum calculating section 3g. The data latch 3h inputs the user data from the keyboard 2 illustrated in FIG. 2. That is, the user data inputted from the keyboard 2 are latched by the data latch 3h and outputted to the P/S shift register 3d and the checksum calculating section 3g.

The hour/minute/second data inputted from the digital timer 1 are supplied to the checksum calculating section 3g which in turn perform the checksum calculation on the basis of the hour/minute/second data and the user data so as to output the calculation result together with data. Further, the drop frame data detecting section 3f detects the time data (except 0, 10, 20, 30, 40 and 50 minutes) corresponding to the drop frame on the basis of the hour/minute/second data and outputs the detection status to the P/S shift register 3a only in the case that the status of the drop frame mode is selected. The data load timing generating section 3e receives the VD pulse as a clock and generates a load pulse after decision of the second data so as to load value to the respective P/S shift registers 3a to 3d. The data which have been loaded are outputted as the CTL data by one bit from the header 3d to the monostable multivibrator 5 illustrated in FIG. 2.

The CTL data recorded on a magnetic tape through the magnetic head 8 illustrated in FIG. 2 is reproduced in accordance with the system disclosed in the Japanese Utility Model Publication No. 57-34633. In the reproducing circuit, an arrangement of the decoder which is responsive to the duty detecting section is illustrated in

6

FIG. 4. In FIG. 4, the CTL data (duty decision value) and CTL pulse inputted from the duty detecting section are inputted into a shift register 9 having a length above 51 bits and the data are latched in accordance with the CTL pulse which is used as a clock. A comparator 11, being coupled to the output side of the shift register 9, successively compares the 11 bits with a header pattern. If agreeing therewith, a latch 10 latches 51st bit data (corresponding to the drop frame bit) at the output side thereof in the coincidence detecting status so as to output it as the drop frame mode status.

Further embodiments of this invention will be described hereinbelow. These embodiments are arranged so as to set a time code (CTLTC) as means for newly recording time data in the CTL coding system. This time code is constructed with 50-bit data, i.e., a header (11 bits), user data (4-bit BCD 4 figures), time code data (BCD 6 figures) and a checksum (4 bits). In the case of a 30-frame-period video signal in the NTSC, dummy bits (10 or 8 bits) are further added to the rear side of the checksum so that the total bit number becomes 60 or 58.

FIG. 5 is a block diagram showing a data recording system according to a second embodiment of this invention. In FIG. 5, illustrated at numeral 21 is a master VTR which records a SMPTE time code and outputs a SMPTE time code signal through a time-code output terminal TCOU when being in the reproducing mode, the SMPTE time code signal from master VTR 21 being fed to an input terminal TCIN of a SMPTE time code reader 22. The time code reader 22 has an arrangement as illustrated in FIG. 6. In FIG. 6, the inputted time code signal is supplied to a clock generator 22a so as to derive a clock signal (generate clocks) from the inputted time code signal and then supply the clock signal to a synchronous word shift register 22b which in turn inputs the time code signal in response to the clock signal therefrom. The synchronous word shift register 22b is coupled to a synchronous detection circuit 22c to detect the synchronizing portion to distinguish between the reading directions of FWD/REV in accordance with the bit information after the synchronous detection to generate a reading direction signal. The reading direction signal generated by the synchronous detection circuit 22c is fed to a data shift register 22d which in turn inputs the time code signal in response to the reading direction signal therefrom.

The clock generator 22a is also coupled through an 80-counter 22e, which counts the clocks up to 80 and then generates a count signal which is in turn supplied to a comparator 22f to compare the count signal in timing with the detection signal from the synchronous detection circuit 22c check whether the data are correct. The comparator 22f outputs a data-reading timing pulse to a buffer shift register 22g which in turn outputs a 64- or 32-bit time code to a data bus buffer 22h for keeping the contents (hour, minute, second, frame) of the time code. The contents of the time code can be read from an external through a data bus by setting a read status Read to low. Further, the data may be arranged to be read out when a data set status INTR which shows that a new time code is read becomes high. This is for preventing the same data from being repeatedly read out. The data set status INTR is set to be low in response to the read status Read being set to be low.

Returning again to FIG. 5, the contents of the time code kept in the data bus buffer 22h of the time code reader 22 are read out by means of a time-code genera-

tor 23. The time-code generator 23 has a time-code counter (hour, minute, second) which is arranged such that the count value becomes equal to the value read by the time-code reader 22. Thus, the time code value read out from the master VTR 21 is synchronously generated by the time-code generator 23. When the frame data and "second" of the generated time code value are 0 second and 10 frames, 2 seconds and 10 frames, 4 seconds and 10 frames, 6 seconds and 10 frames, and 8 seconds and 10 frames, the time code generator 23 supplies a writing start signal and a writing time code value to a CTL data output circuit 4. Here, only the hour/minute/second data obtained by adding 2 seconds to the time code value at that time are recorded, and the address of the frame data are not recorded. The 10 frames correspond to 10 dummy bits, and in the case of PAL whose frame frequency is 25 Hz, the supply is not required, and in response to 0 second (0 frame), 2 seconds and 4 seconds, the writing time code is supplied.

The CTL data output circuit 24 starts to output the data in order from the leading bit of the header in the next frame in response to the writing start signal. Here, the time code value to be outputted is the data just supplied from the time-code generator 23. The outputted CTL data are led to a slave VTR 25 so as to be used as a duty-variable signal comprising recording control pulses.

More specifically, in the data recording system illustrated in FIG. 5, the SMPTE time code reader 22 detects a first time code (i.e., the CTL time code) assigned to the respective television frame, and the time code generator 23 generates on the basis of this detection result, a second time code (e.g. the CTL time code), so that the first time code for each of the frames of the television signal is converted into the second time code for a plurality of frames and is recorded as variation of the duty ratio of the control signal on a control track through the CTL data output circuit 24. Thus, the SMPTE time code recorded on a master tape becomes coincident in units of frame with the time code recorded on a tape of the slave VTR 25 in accordance with the CTL coding system, and operation under the time code is also allowed at the slave VTR 25 side, and further the data can be used at the master side.

Here, in the above-mentioned conversion dubbing system from the SMPTE time code to the CTL time code, if the VITC (Vertical Interval Time Code) is used instead of the SMPTE time code, the SMPTE time code reader 22 is changed to a VITC reader and the TC terminal connection is changed to a VIDEO connection.

FIG. 7 is a block diagram showing a data recording system according to a third embodiment of this invention, where a CTL time code recorded in a master VTR is read out in reproduction and a SMPTE time code synchronously generated is recorded in a slave VTR. In FIG. 7, when a master VTR 26 is in the reproducing mode, a CTL pulse outputted from a CTL pulse output terminal is supplied to a CTL pulse input terminal of a CTLTC decoder 27. The CTLTC decoder 27 has an arrangement as illustrated in FIG. 8. The decision of the duty ratio of the inputted CTL pulse is made by means of a CTL duty decision circuit 27a. The CTL data comprising "0" and "1" are extracted and, together with CTL clock, supplied to a time code data extracting circuit 27b. The time code extracting circuit 27b latches the CTL data and detects the header to extract the time code data and further checks the drop frame bit in the

latched data to output the decision status of the drop frame bit and still further supplies the latched data to a data buffer 27c. In response to the data being set, the data buffer 27c sets the data set status INTR to the high level, and in response to the low level being applied to the data output enabling input (Read), outputs the time code data to the parallel data output and then resets the data set status INTR to low.

Returning again to FIG. 7, a time code generator 28 which receives the output of the CTLTC decoder 27 has an arrangement as illustrated in FIG. 9. A time-code reading control circuit receives the output of the CTLTC decoder 27 so as to supply it as a preset value to a time code counter 28b which in turn starts the counting operation in response thereto. The counter 28b counts up every frame. Here, one time code is assigned for one frame. The count value (time code data) is converted into a serial data by means of a serializing circuit 28c and then outputted to a time-code output terminal TCOUT in synchronism with an external synchronizing signal EXTSYNC. This output is supplied to a time-code input terminal TCIN of a slave VTR 29 illustrated in FIG. 7 so as to be recorded in a time code track of a slave tape when being in the recording mode.

Accordingly, in the third embodiment described with reference to FIGS. 7 to 9, the CTL time code recorded in the control track for a period of a plurality of TV frames is detected by means of the CTLTC decoder 27, and a new time code relative to each TV frame (for example, the SMPTE time code) is generated on the basis of this detection result by means of the time-code generator 28 and then recorded in the cue track or video track so as to be positioned in the vertical blanking of the television signal. Here, in the case that the above-mentioned conversion dubbing system from the CTL time code to the SMPTE time code is used for the VITC, the time-code generator 28 is required to further have an encoder 28d and an inserter 28e for inserting the code signal into the video signal, as illustrated in FIG. 9.

It should be understood that the foregoing relates to only preferred embodiments of the present invention, and that it is intended to cover all changes and modifications of the embodiments of the invention herein used for the purposes of the disclosure, which do not constitute departures from the spirit and scope of the invention.

What is claimed is:

1. In a data recording system for a video tape recorder which records control pulses in a control track of a magnetic tape of said video tape recorder with the duty cycle of said control pulses being changed in accordance with data relating to said magnetic tape, the improvement comprising:

means for adding dummy bits to a data block including said control pulses, said adding means adds said dummy bits at an end position of said data block, the leading bit of said dummy bits represents the number of said dummy bits and is in a predetermined position relation to the first bit of said data block; and

means for changing the number of said dummy bits at a predetermined period.

2. A data recording system as claimed in claim 1, wherein said adding means adds a predetermined number of said dummy bits to said data block and said changing means changes the predetermined number of said dummy bits to be reduced by a predetermined number at said predetermined period thereby to match

a time code represented by said data block with real time.

3. A data recording system as claimed in claim 1, wherein said adding means adds said dummy bits at a position following a time code contained in said data block.

4. In a data recording system for a video tape recorder including means for recording control pulses in a control track of a magnetic tape and modulating means for pulse width modulating said control pulses in accordance with data relating to said magnetic tape, the improvement comprising:

means for adding dummy bits to a data block including said control pulses;

means for periodically changing the number of said dummy bits at a predetermined period thereby to synchronize a time code included in said data block with real time; and

means for controlling said modulating means to modulate a first bit of said dummy bits to identify the number of said dummy bits added to said data block.

5. An improved data recording system in accordance with claim 4, wherein said adding means adds said dummy bits at a position in said data block following bits representing a checksum in said data block.

6. An improved data recording system in accordance with claim 4, wherein said changing means controls said

adding means for periodically reducing a number of said added dummy bits.

7. In a data recording system for a video tape recorder including means for recording control pulses in a control track of a magnetic tape and modulating means for pulse width modulating said control pulses in accordance with data relating to said magnetic tape, the improvement comprising:

first means for adding dummy bits to a data block including said control pulses;

second means for periodically controlling said first means to periodically change the number of said added dummy bits at a predetermined period; and

third means for controlling said modulating means to modulate a predetermined bit of said data block to represent the number of said added dummy bits, said predetermined bit having a predetermined position relative to a first bit of said data block, said third means controls said modulating means to modulate the first bit of said dummy bits to identify the number of said added dummy bits.

8. An improved data recording system in accordance with claim 7, wherein said first means adds said dummy bits at a position in said data block following bits representing a time code in said data block.

9. An improved data recording system in accordance with claim 7, wherein said second means controls said first means for periodically reducing the number of said added dummy bits thereby to synchronize a time code included in said data block with real time.

* * * * *

35

40

45

50

55

60

65



US006104858A

United States Patent [19]

Suzuki

[11] Patent Number: 6,104,858
[45] Date of Patent: Aug. 15, 2000

[54] APPARATUS FOR REPRODUCING A VIDEO SIGNAL AND A CORRECTIVE SIGNAL AND FOR CORRECTING THE VIDEO SIGNAL IN RESPONSE TO THE CORRECTIVE SIGNAL

[75] Inventor: Koji Suzuki, Yokohama, Japan

[73] Assignee: Victor Company of Japan, Ltd.,
Yokohama, Japan

[21] Appl. No.: 08/852,816

[22] Filed: May 7, 1997

Related U.S. Application Data

[62] Division of application No. 08/309,822, Sep. 21, 1994, Pat. No. 5,646,795.

[30] Foreign Application Priority Data

Sep. 30, 1993 [JP] Japan 5-268306

[51] Int. Cl.⁷ H04N 5/76

[52] U.S. Cl. 386/65; 386/95; 386/113

[58] Field of Search 386/46, 52, 53,
386/65, 60, 85, 69, 73, 95, 113, 86, 47;
H04N 5/76, 5/94

[56] References Cited

U.S. PATENT DOCUMENTS

5,091,899 2/1992 Adachi et al. 386/65
5,287,224 2/1994 Tsuchiya et al. 386/65
5,463,505 10/1995 Kaniwa et al. 386/65

OTHER PUBLICATIONS

"The Specification of Consumer HD-VTR", Keitaro Yamashita et al., ITEJ Technical Report vol. 15, No. 50, Sep. 26, 1991.

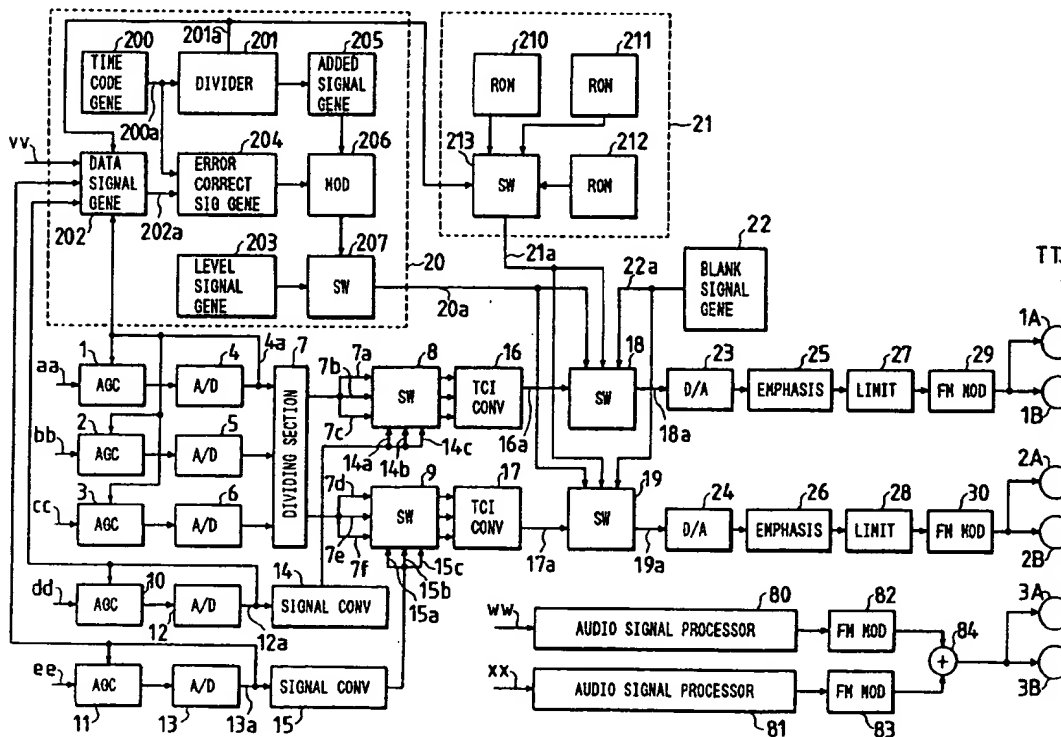
Primary Examiner—Huy T. Nguyen

Attorney, Agent, or Firm—Lowe Hauptman Gopstein Gilman & Berner

[57] ABSTRACT

A video signal is divided into a plurality of partial signals. A time code signal is generated which is incremented every field or frame of the video signal. One of predetermined different corrective signals or calibration signals is sequentially selected in response to the time code signal. The time code signal and the selected corrective signal are interposed in segments of the partial signals which relate to a given line of the field or frame to convert the partial signals into composite signals. The composite signals are recorded on the recording medium.

3 Claims, 11 Drawing Sheets



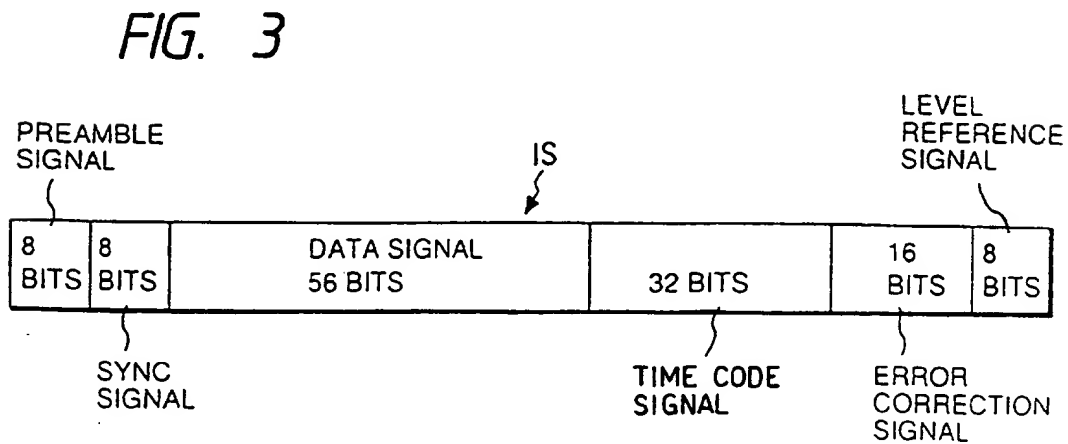
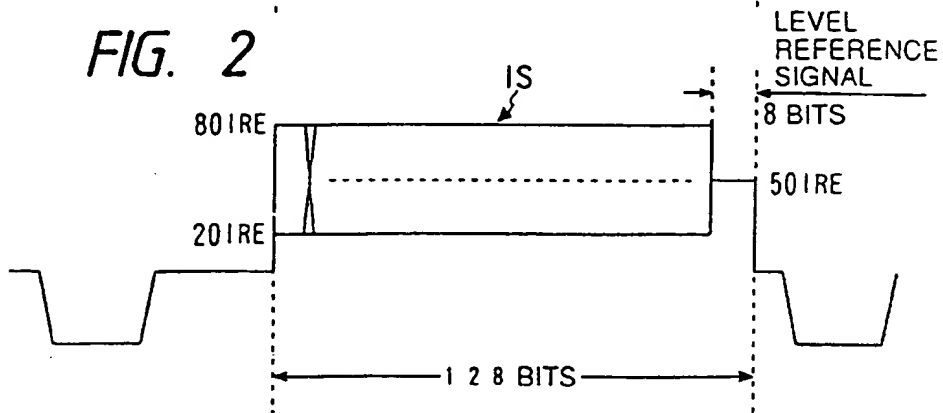
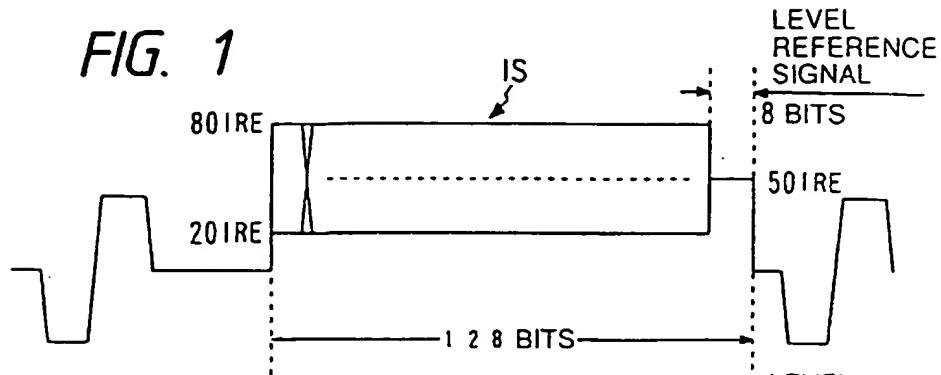


FIG. 4

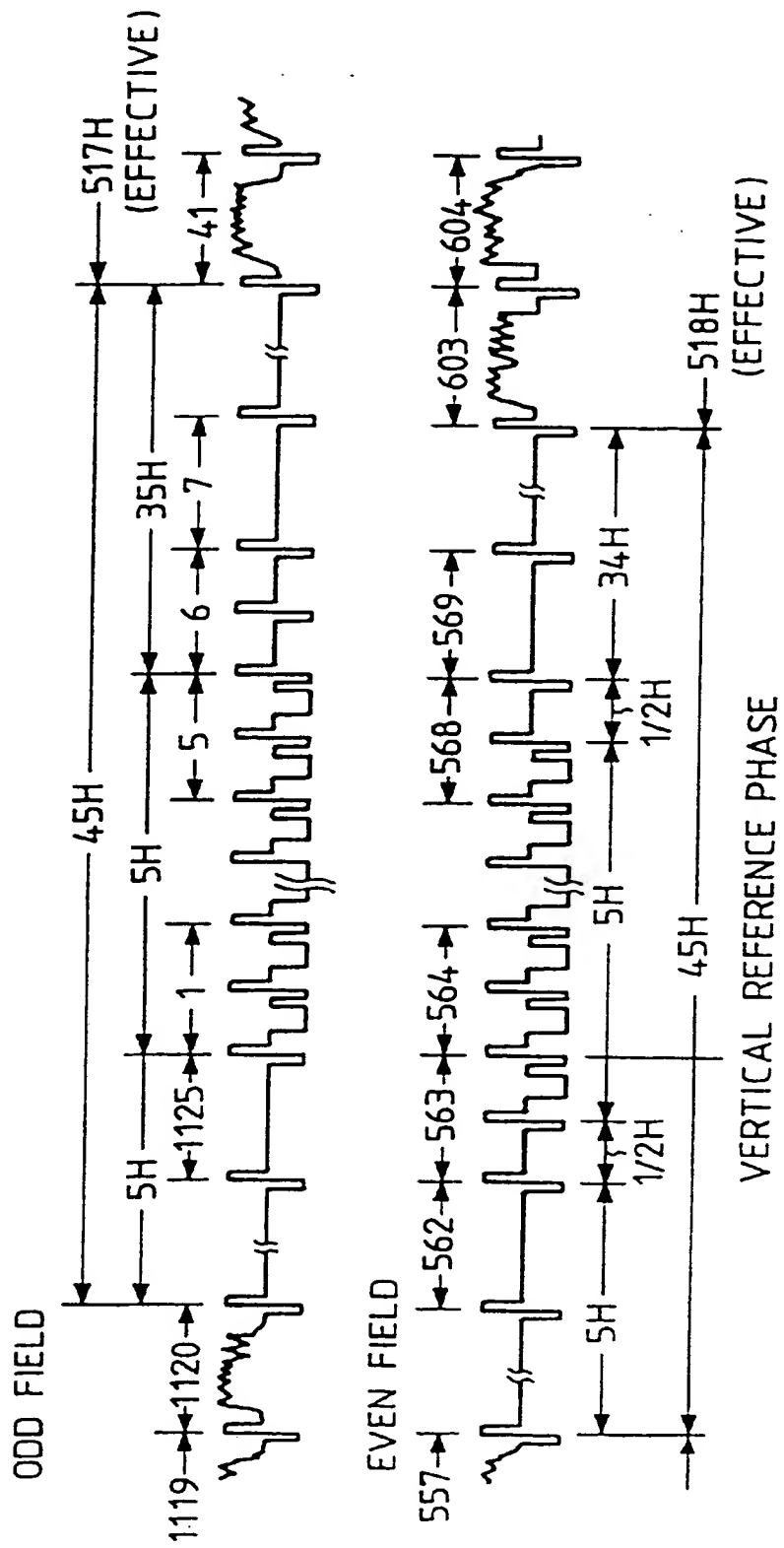


FIG. 5

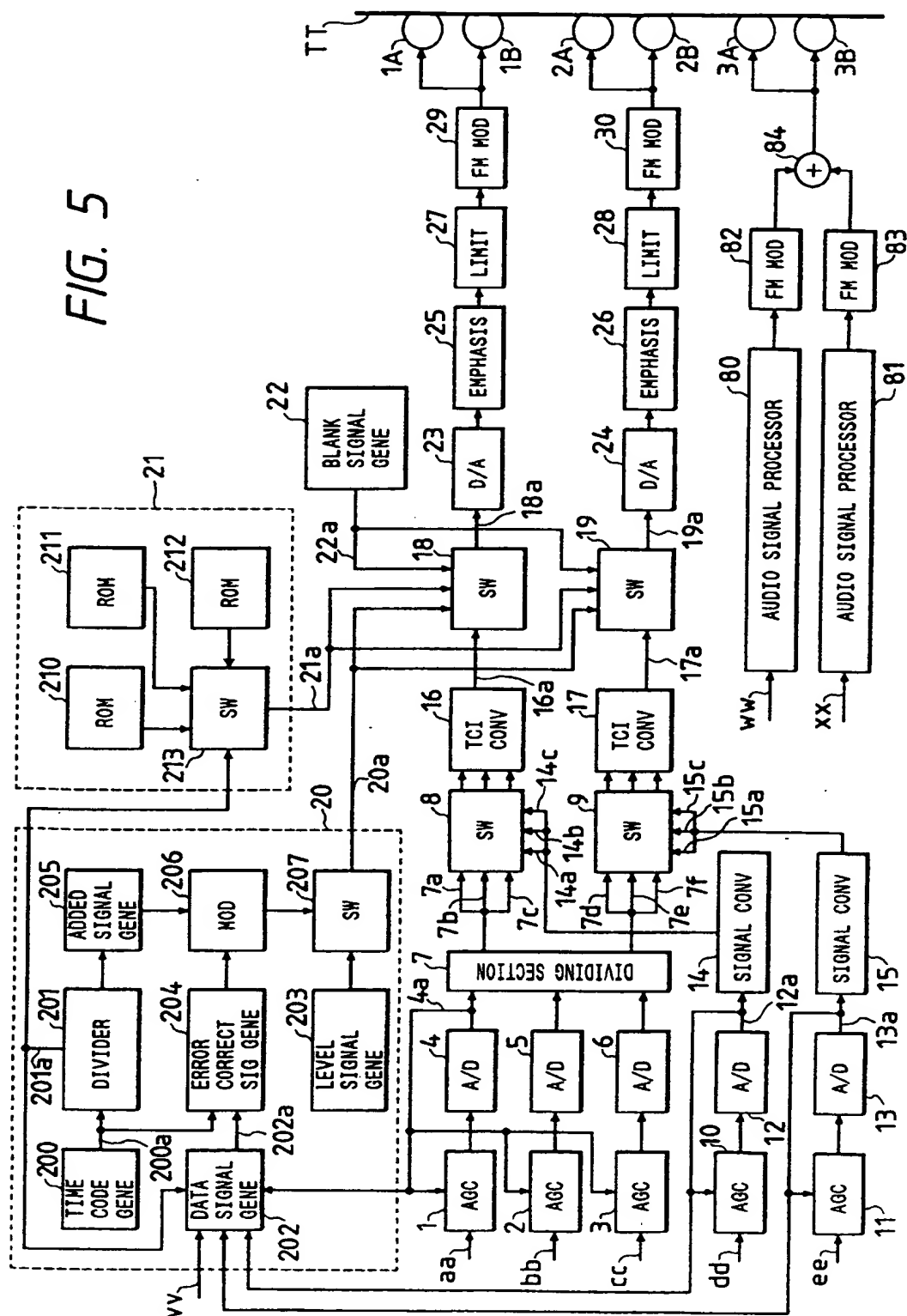


FIG. 6

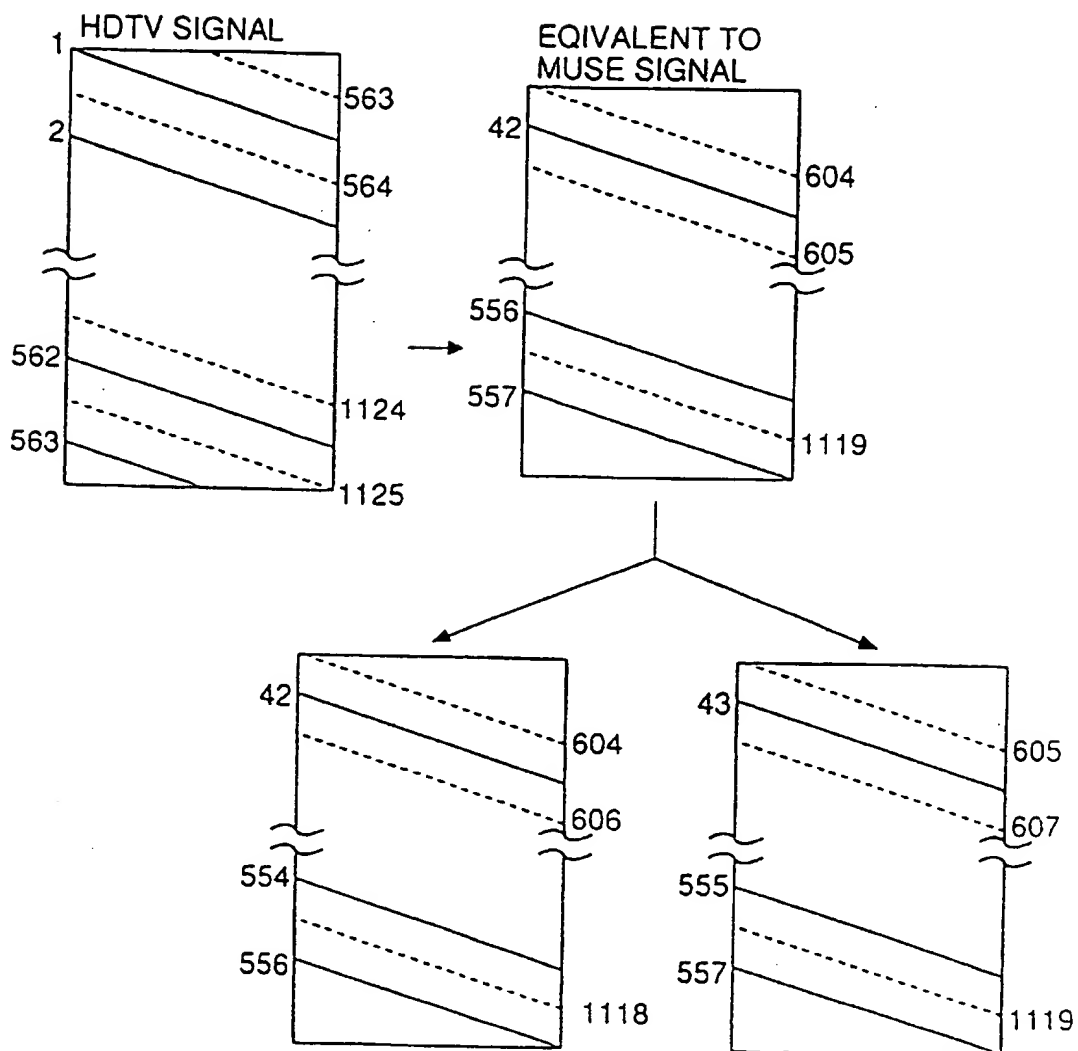


FIG. 7

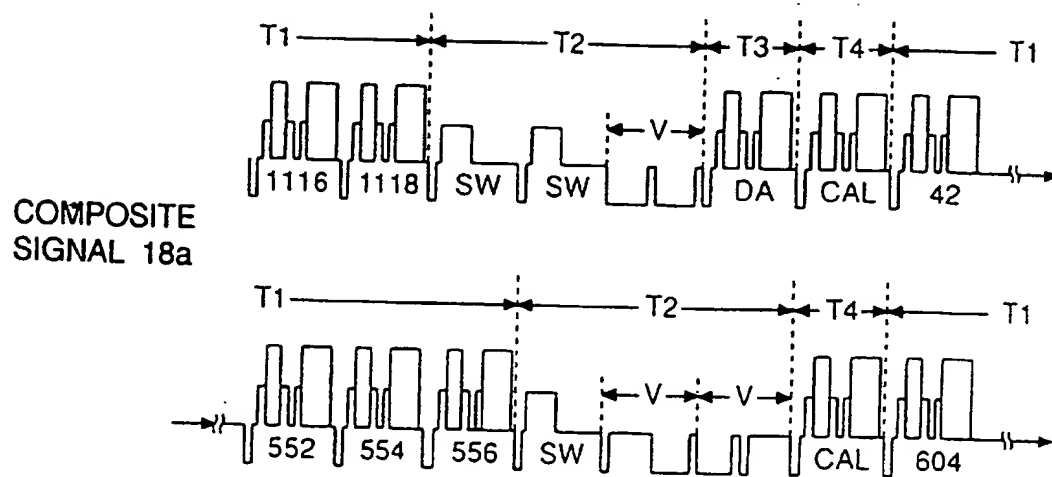


FIG. 8

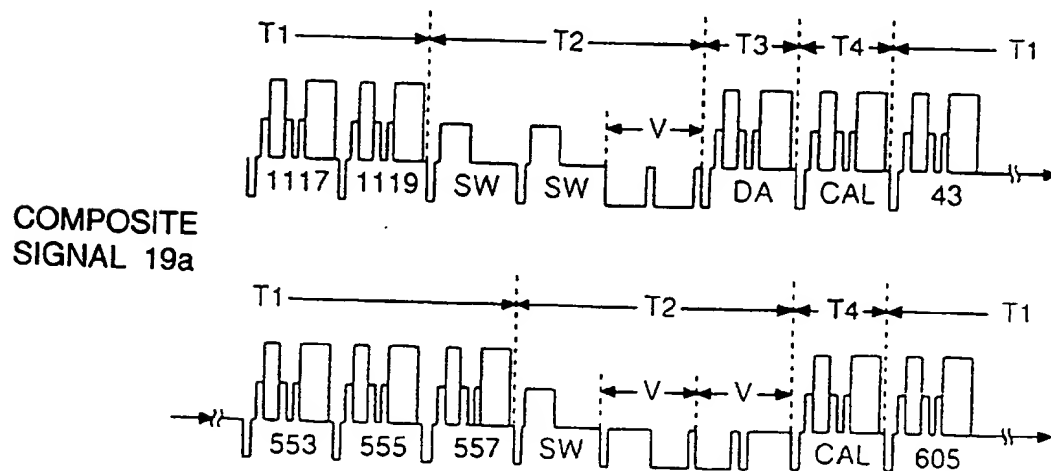


FIG. 9

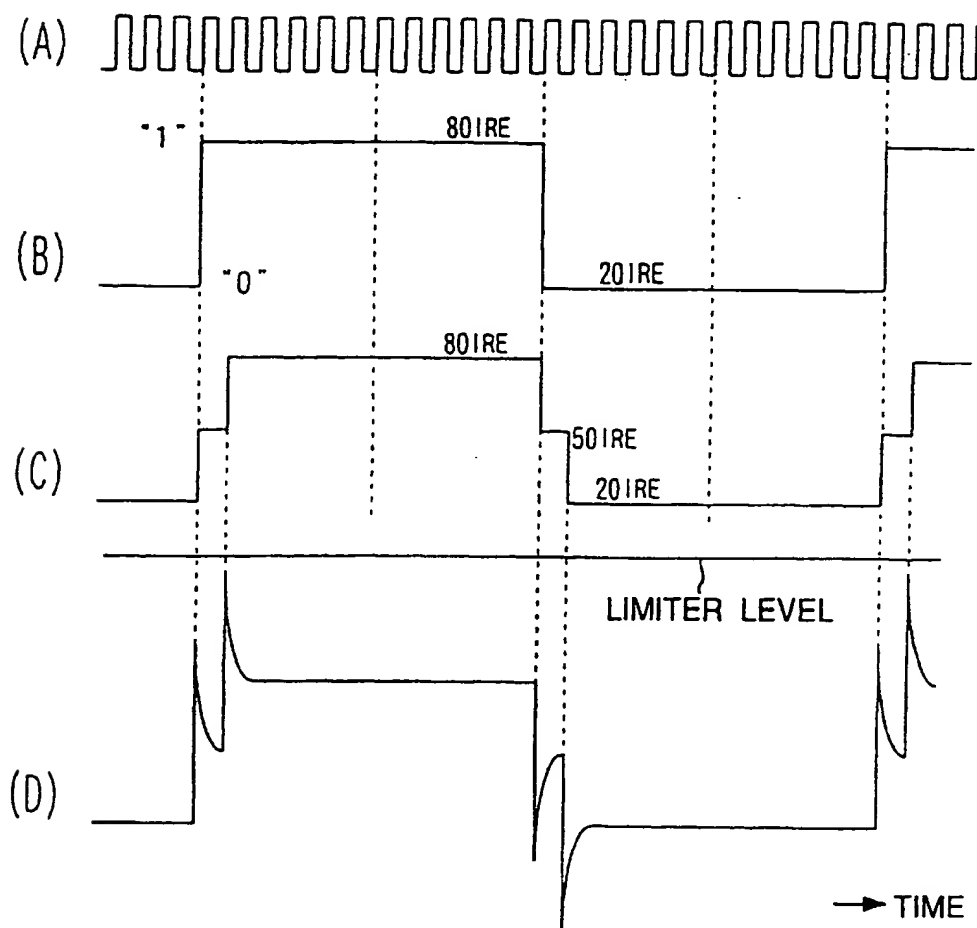


FIG. 10

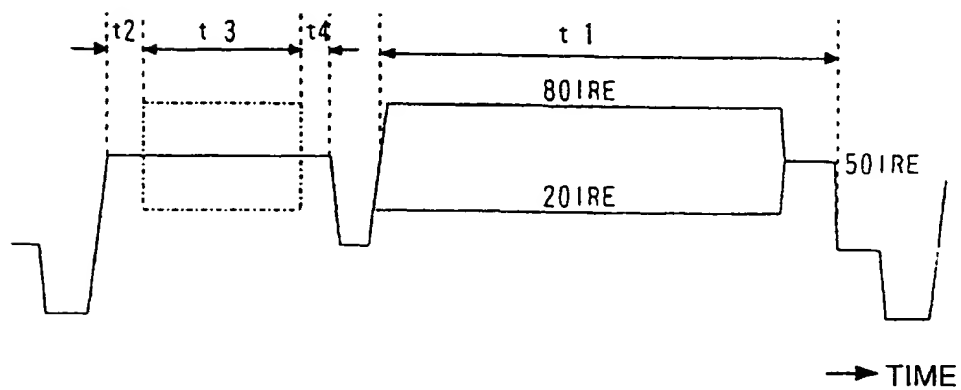


FIG. 11

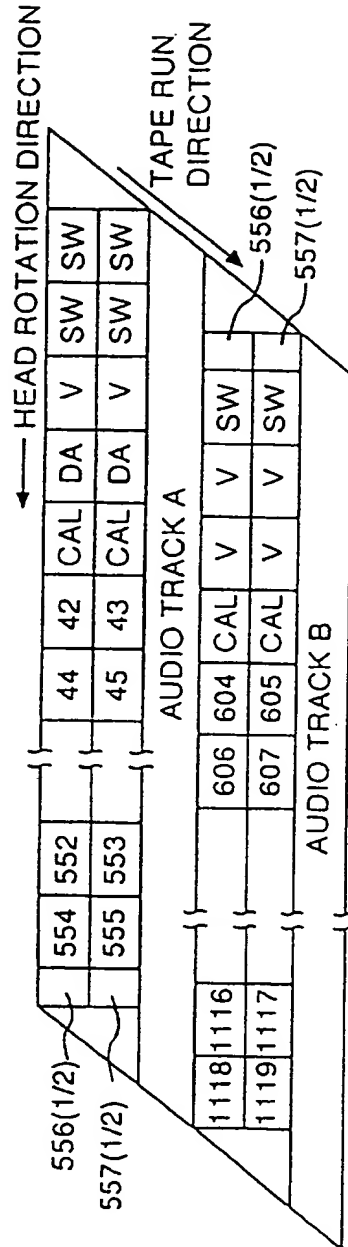


FIG. 12

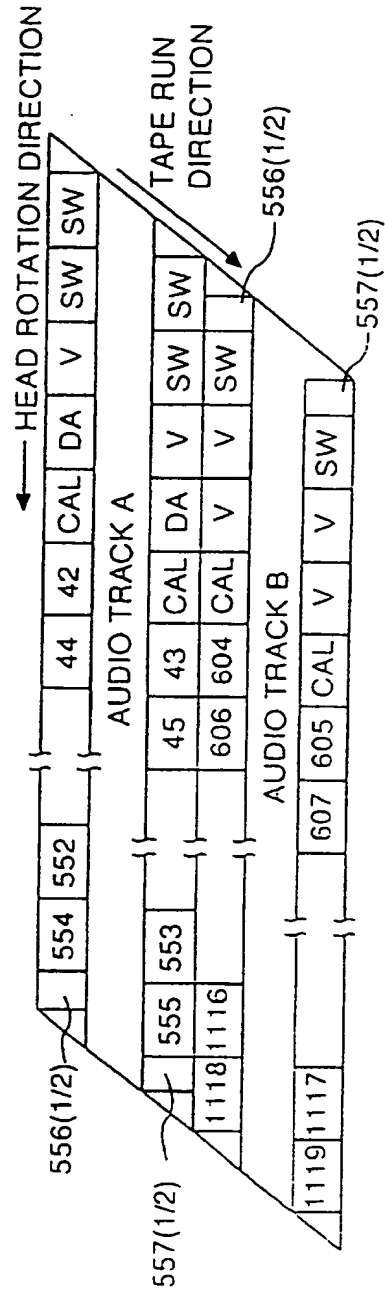


FIG. 13

FIRST FIELD

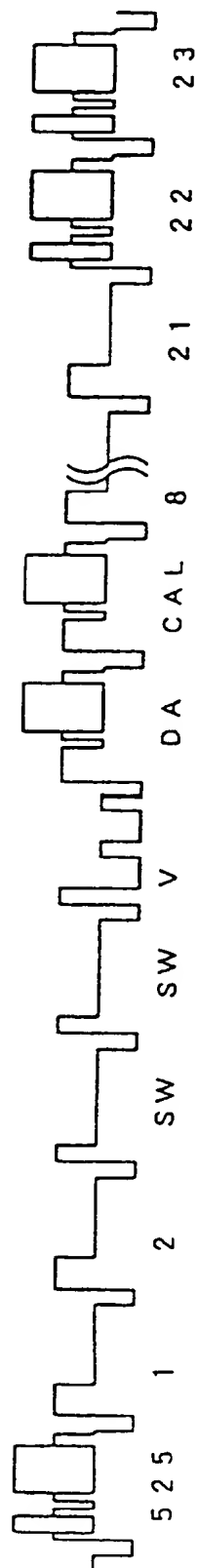
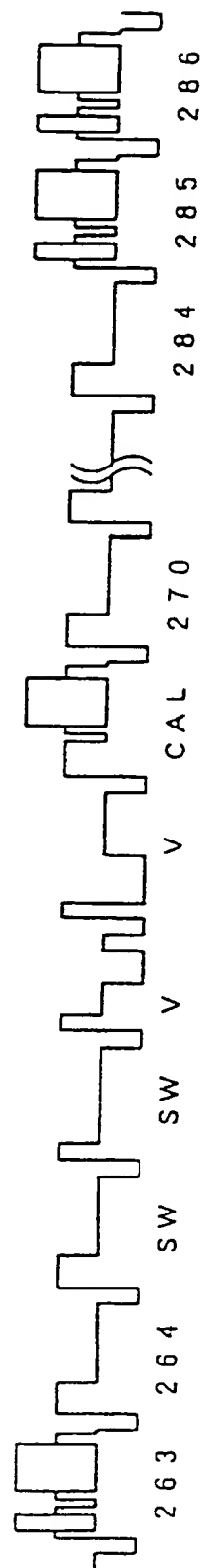


FIG. 14

SECOND FIELD



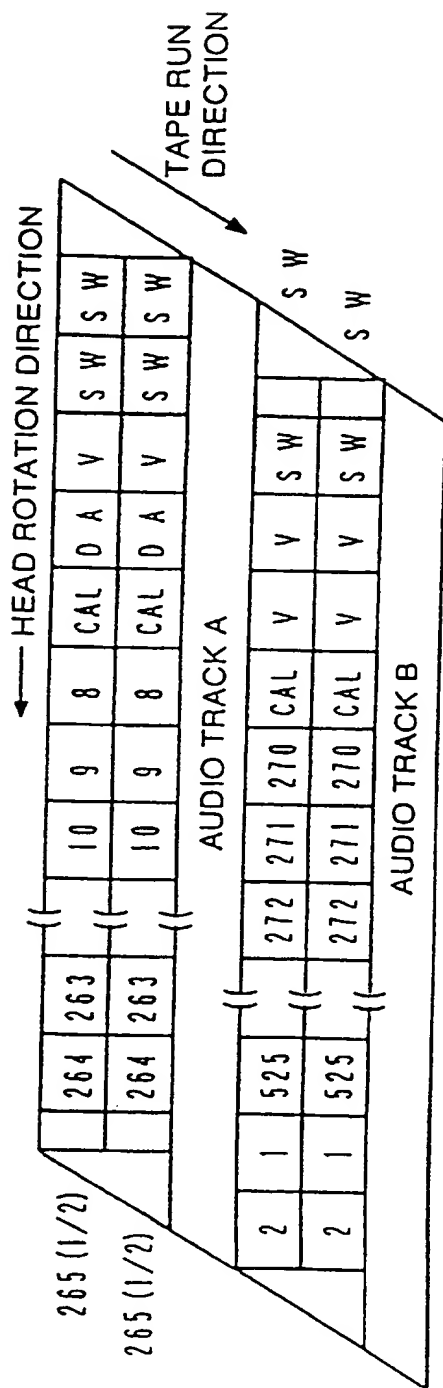


FIG. 15

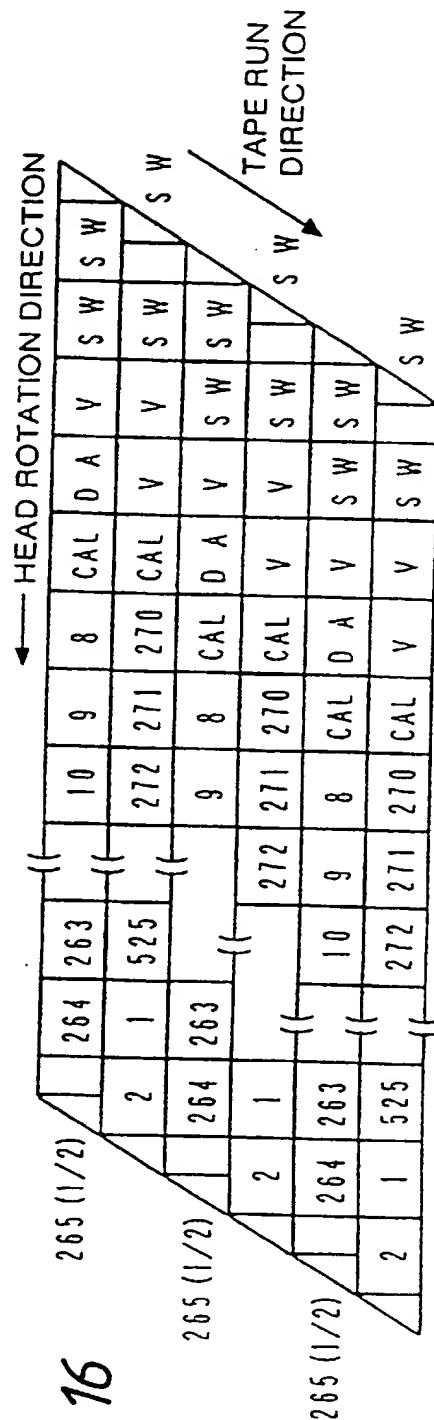


FIG. 16

FIG. 17

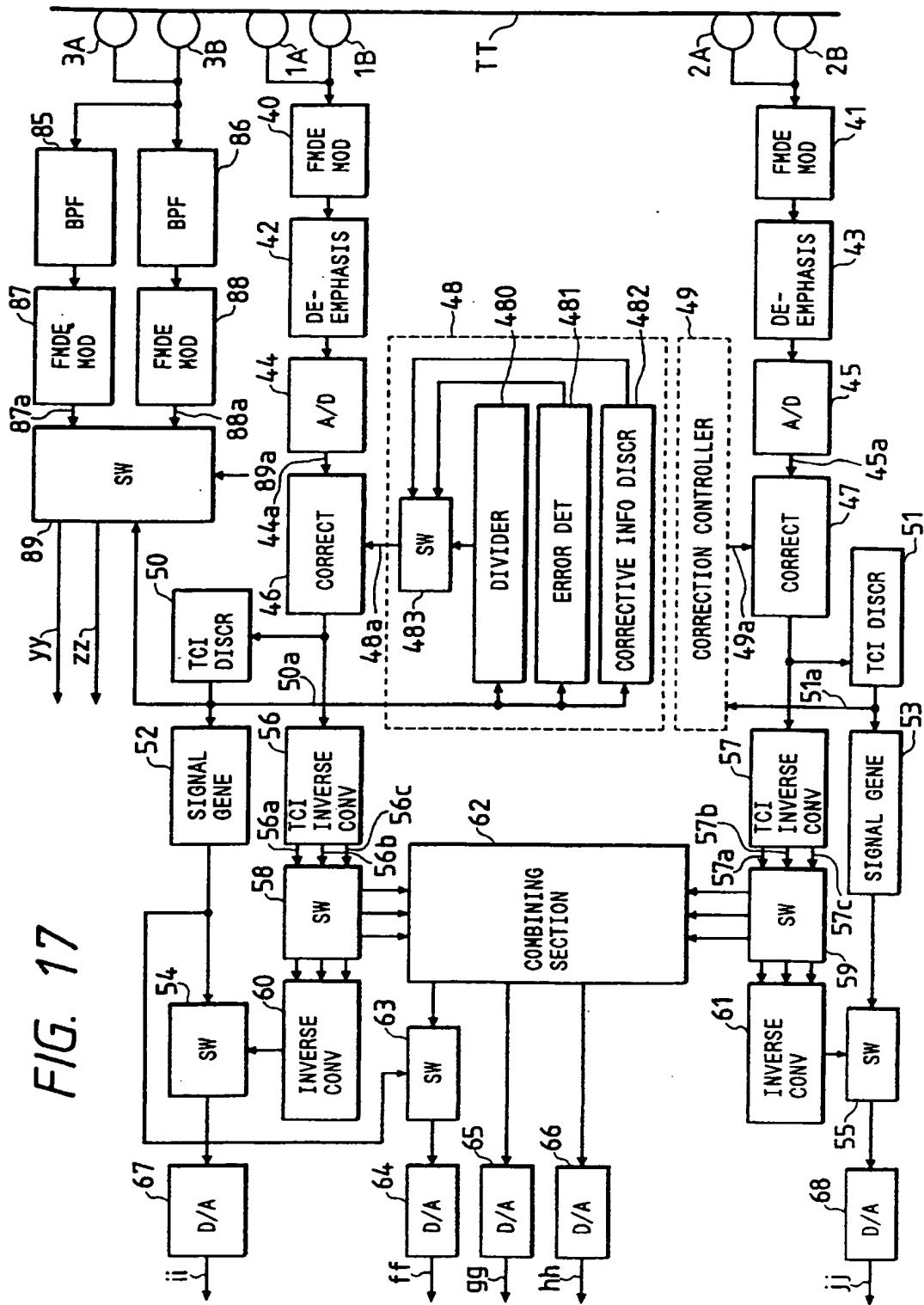


FIG. 18

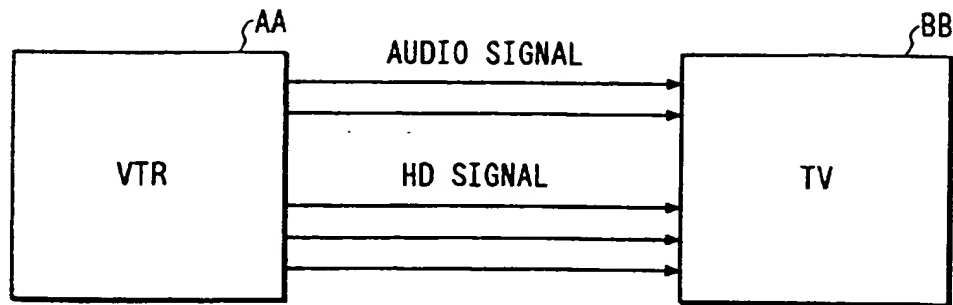


FIG. 19

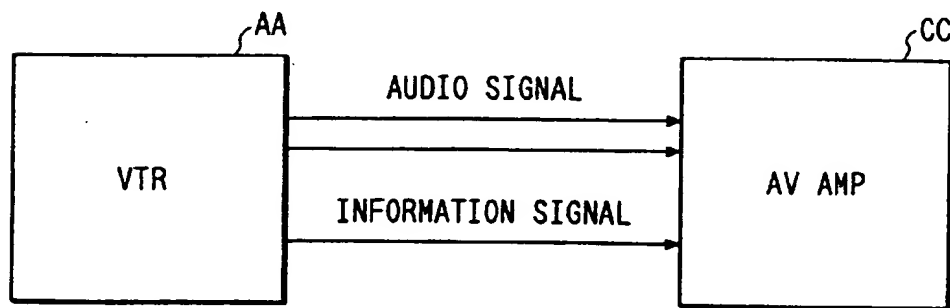
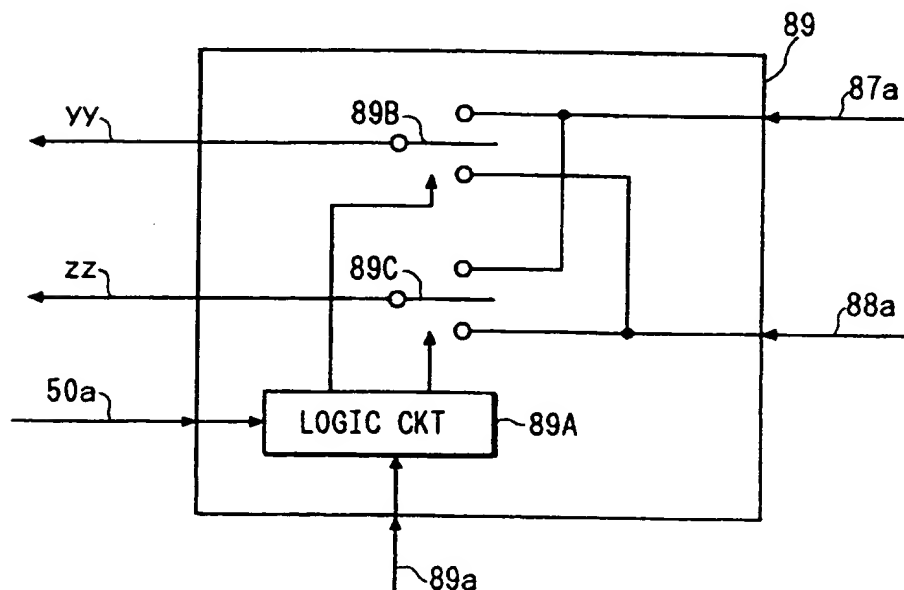


FIG. 20



APPARATUS FOR REPRODUCING A VIDEO SIGNAL AND A CORRECTIVE SIGNAL AND FOR CORRECTING THE VIDEO SIGNAL IN RESPONSE TO THE CORRECTIVE SIGNAL

This application is a division of application Ser. No. 08/309,822 filed Sep. 21, 1994, U.S. Pat. No. 5,646,795.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a signal recording apparatus and a signal reproducing apparatus. This invention also relates to a recording medium such as a magnetic tape.

2. Description of the Prior Art

One type of high-density magnetic recording of a video signal is segment recording in which every frame represented by the video signal is divided into a plurality of segments recorded on tracks on a magnetic tape via magnetic heads respectively. During a playback process, the recorded signal segments are reproduced from the tracks via the magnetic heads respectively. Generally, there are a plurality of signal processors related to the respective signal segments. During the playback process, a variation in characteristics among the signal processors causes a line flicker or a field flicker in indicated pictures generated from the reproduced signal segments.

An advanced high-vision VTR (video tape recorder) is designed to solve the above-indicated flicker problem (see ITFJ Technical Report, Vol. 15, No. 50, pp 1-6, Sep. 1991). The advanced high-vision VTR generates a plurality of corrective signals (calibration signals) designed to compensate for a variation in characteristics among signal processors. The corrective signals are recorded on starting portions of tracks on a magnetic tape. During a playback process, the corrective signals are reproduced from the tracks, and compensation for the variation in characteristics among the signal processors is executed in response to the reproduced corrective signals.

The advanced high-vision VTR has a problem such that recording of the corrective signals reduces the efficiency of use of the magnetic tape with respect to video information.

Some of magnetic recording and reproducing apparatus are of the deep-layer recording type in which an FM audio signal is recorded into a deep layer portion of a magnetic tape while a video signal, which results from frequency-multiplexing an FM luminance signal and frequency-down-converted color signals, is recorded on the magnetic tape.

Generally, an audio signal is of various types or modes such as a monophonic mode, a stereophonic mode, and a two-channel mode. An example of the two-channel mode is a bilingual mode in which main-channel information contains Japanese voices while sub-channel information contains English voices.

When such a two-channel audio signal is reproduced from a magnetic tape by the above-indicated apparatus of the deep-layer recording type, Japanese and English voices are simultaneously generated from loudspeakers in the apparatus. In such a case, the user is required to handle a manual switch in the apparatus to select desired one of the Japanese information and the English information.

SUMMARY OF THE INVENTION

It is a first object of this invention to provide an improved signal recording apparatus.

It is a second object of this invention to provide an improved signal reproducing apparatus.

It is a third object of this invention to provide an improved magnetic tape.

A first aspect of this invention provides an apparatus for dividing a video signal into a plurality of partial signals and recording the partial signals on a recording medium which comprises means for generating a time code signal incremented every field or frame of the video signal; means for sequentially selecting one of predetermined different corrective signals in response to the time code signal; means for interposing the time code signal and the selected corrective signal in segments of the partial signals which relate to a given line of the field or frame to convert the partial signals into composite signals; and means for recording the composite signals on the recording medium.

A second aspect of this invention provides an apparatus for dividing a video signal into a plurality of partial signals and recording the partial signals on a recording medium which comprises means for generating a time code signal representing a time code number incremented every field or frame of the video signal; means for dividing the time code number by a predetermined natural number Q equal to or greater than 2, and generating a signal representing a remainder of the dividing; means for sequentially selecting one of predetermined R different corrective signals in response to the remainder-representing signal, wherein R denotes a predetermined natural number equal to or smaller than the number Q ; means for interposing the time code signal and the selected corrective signal in segments of the partial signals which relate to a given line of the field or frame to convert the partial signals into composite signals; and means for recording the composite signals on the recording medium.

A third aspect of this invention provides an apparatus for dividing a video signal into a plurality of partial signals and recording the partial signals on a recording medium which comprises means for selecting one of predetermined different corrective signals; means for generating an information signal representing a presence and an absence of the selected corrective signal; means for interposing the selected corrective signal and the information signal in segments of the partial signals which relate to a given line of a field or frame of the video signal to convert the partial signals into composite signals; and means for recording the composite signals on the recording medium.

A fourth aspect of this invention provides an apparatus for dividing a video signal into a plurality of partial signals and recording the partial signals on a recording medium which comprises means for generating a time code signal representing a time code number incremented every field or frame of the video signal; means for dividing the time code number by a predetermined natural number Q equal to or greater than 2, and generating a signal representing a remainder of the dividing; means for sequentially selecting one of predetermined R different corrective signals in response to the remainder-representing signal, wherein R denotes a predetermined natural number equal to or smaller than the number Q ; means for generating an information signal representing a presence and an absence of the selected corrective signal; means for interposing the time code signal, the information signal, and the selected corrective signal in segments of the partial signals which relate to a given line of the field or frame to convert the partial signals into composite signals; and means for recording the composite signals on the recording medium.

It is preferable that the apparatus further comprises means for extracting audio identification information from the

video signal, the audio identification information representing a type of an audio signal related to the video signal, and means for adding the audio identification information to the information signal.

A fifth aspect of this invention provides a magnetic tape having a plurality of tracks extending in directions oblique thereto, the tracks storing partial signals composing a video signal, the tracks storing a time code signal incremented every field or frame of the video signal, the tracks storing a corrective signal sequentially selected from among predetermined different corrective signals, the time code signal and the selected corrective signal being interposed in segments of the partial signals which relate to a given line of the field or frame.

A sixth aspect of this invention provides a magnetic tape having a plurality of tracks extending in directions oblique thereto, the tracks storing partial signals composing a video signal, the tracks storing a corrective signal selected from among predetermined different corrective signals, the tracks storing an information signal representing a presence and an absence of the selected corrective signal, the selected corrective signal and the information signal being interposed in segments of the partial signals which relate to a given line of a field or frame of the video signal.

A seventh aspect of this invention provides a video signal reproducing apparatus comprising means for reproducing a video signal from a recording medium, the video signal containing a time code signal and a corrective signal, the time code signal being incremented every field or frame of the video signal, the corrective signal being sequentially selected from among predetermined different corrective signals in response to the time code signal; means for extracting the time code signal from the reproduced video signal; means for identifying the corrective signal in the reproduced video signal in response to the extracted time code signal; and means for correcting the reproduced video signal in response to a result of said identifying.

An eighth aspect of this invention provides a video signal reproducing apparatus comprising means for reproducing a video signal from a recording medium, the video signal containing a time code signal and a corrective signal, the time code signal being incremented every field or frame of the video signal, the corrective signal being sequentially selected from among predetermined R different corrective signals in response to a remainder of dividing a number represented by the time code signal by a predetermined natural number Q equal to or greater than 2, wherein R denotes a predetermined natural number equal to or smaller than the number Q; means for extracting the time code signal from the reproduced video signal; means for dividing the number represented by the time code signal by the number Q, and generating a signal representing a remainder of said dividing; means for identifying the corrective signal in the reproduced video signal in response to the remainder-representing signal; and means for correcting the reproduced video signal in response to a result of said identifying.

A ninth aspect of this invention provides a video signal reproducing apparatus comprising means for reproducing a video signal from a recording medium, the video signal containing a corrective signal and an information signal, the corrective signal being selected from among predetermined different corrective signals, the information signal representing a presence and an absence of the corrective signal; means for extracting the information signal from the reproduced video signal; means for extracting the corrective signal from the reproduced video signal; means for correct-

ing the reproduced video signal in response to the corrective signal when the extracted information signal represents the presence of the corrective signal; and means for non-correcting the reproduced video signal when the extracted information signal represents the absence of the corrective signal.

A tenth aspect of this invention provides a video signal reproducing apparatus comprising means for reproducing a video signal from a recording medium, the video signal containing a time code signal and a corrective signal, the video signal further containing an information signal representing a presence and an absence of the corrective signal, the time code signal being incremented every field or frame of the video signal, the corrective signal being sequentially selected from among predetermined R different corrective signals in response to a remainder of dividing a number represented by the time code signal by a predetermined natural number Q equal to or greater than 2, wherein R denotes a predetermined natural number equal to or smaller than the number Q; means for extracting the time code signal from the reproduced video signal; means for extracting the information signal from the reproduced video signal; means for dividing the number represented by the time code signal by the number Q, and generating a signal representing a remainder of said dividing; means for identifying the corrective signal in the reproduced video signal in response to the remainder-representing signal and the extracted information signal; and means for correcting the reproduced video signal in response to a result of said identifying.

It is preferable that the apparatus further comprises means for reproducing an audio signal from the recording medium, means for extracting an audio identification signal from the reproduced video signal, the audio identification signal representing a type of the audio signal, means for outputting the reproduced audio signal in a changeable format, and means for setting said format in response to the audio identification signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram of the waveform of an information signal.

FIG. 2 is a diagram of the waveform of an information signal.

FIG. 3 is a diagram of the format of the information signals in FIGS. 1 and 2.

FIG. 4 is a diagram of the waveform of a high-definition television signal.

FIG. 5 is a block diagram of a recording side of a signal recording and reproducing apparatus according to an embodiment of this invention.

FIG. 6 is a flow diagram of operation of a dividing section in the apparatus of FIG. 5.

FIG. 7 is a diagram of the waveform of an even-line video signal in which a TCI information signal, a corrective signal, and other signals are interposed.

FIG. 8 is a diagram of the waveform of an odd-line video signal in which a TCI information signal, a corrective signal, and other signals are interposed.

FIG. 9 is a diagram of the waveforms of various signals in the apparatus of FIG. 5.

FIG. 10 is a diagram of the waveform of a TCI information signal in the apparatus of FIG. 5.

FIG. 11 is a diagram of a signal record pattern on a magnetic tape which occurs during a W mode of operation of the apparatus in FIG. 5.

FIG. 12 is a diagram of another signal record pattern on a magnetic tape which occurs during the W mode of operation of the apparatus in FIG. 5.

FIG. 13 is a diagram of the waveform of a first-field video signal in which a TCI signal, a corrective signal, and other signals are interposed.

FIG. 14 is a diagram of the waveform of a second-field video signal in which a corrective signal, and other signals are interposed.

FIG. 15 is a diagram of a signal record pattern on a magnetic tape which occurs during a 2NT mode of operation of the apparatus in FIG. 5.

FIG. 16 is a diagram of a signal record pattern on a magnetic tape which occurs during a W-NT mode of operation of the apparatus in FIG. 5.

FIG. 17 is a block diagram of a reproducing side of the signal recording and reproducing apparatus according to the embodiment of this invention.

FIG. 18 is a block diagram of a combination of a VTR (video tape recorder) and a television set.

FIG. 19 is a block diagram of a combination of a VTR (video tape recorder) and an AV amplifier.

FIG. 20 is a block diagram of a switch in the apparatus of FIG. 17.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An apparatus according to an embodiment of this invention can record and reproduce either a combination of a high-definition video signal and an audio signal or a combination of a normal-definition video signal and an audio signal into and from a recording medium. The apparatus according to the embodiment of this invention will be also referred to as the signal recording and reproducing apparatus. A television signal of an HD (high definition) format, which is referred to as an HD signal, is used as an example of the combination of the high-definition video signal and the audio signal. A television signal of an NTSC format, which is referred to as an NTSC signal, is used as an example of the combination of the normal-definition video signal and the audio signal.

The signal recording and reproducing apparatus outputs an HD signal or an NTSC signal which contains an information signal at its time segment corresponding to a given line or lines of every frame (or field). The signal recording and reproducing apparatus receives and accepts such an information-signal-added HD signal or an information-signal-added NTSC signal.

Information Signal

FIG. 1 shows an information signal IS which is interposed in a Y signal (a luminance signal) of the HD format at its time segment corresponding to a given line or lines of every frame (or field). FIG. 2 shows an information signal IS which is interposed in a Y signal (a luminance signal) of the NTSC format at its time segment corresponding to a given line or lines of every frame (or field). Each of the information signals IS of FIGS. 1 and 2 has a digital-signal portion and an analog-signal portion. The digital-signal portion precedes the analog-signal portion. The digital-signal portion has a sequence of 120 bits each changeable between 20 IRE and 80 IRE which correspond to logic levels of "0" and "1" respectively. The analog-signal portion occupies an interval corresponding to 8 bits. The analog-signal portion represents a level reference signal which has a constant level normally corresponding to 50 IRE.

As shown in FIG. 3, each information signal IS has a sequence of an 8-bit preamble signal, an 8-bit sync signal, a 56-bit data signal, a 32-bit time code signal, a 16-bit error correction signal, and the level reference signal. The preamble signal, the sync signal, the data signal, the time code signal, and the error correction signal compose the previously-indicated digital-signal portion of the information signal IS. The preamble signal is used in providing synchronism with a clock signal during reproduction. The sync signal is used in discriminating a start of data (a start of the data signal). The data signal represents information such as the type of the related television signal (the currently-handled television signal). The time code signal represents time information. The error correction signal is used in detecting and correcting signal errors during reproduction. The level reference signal is used in controlling a recording level.

The data signal in the information signal IS has a sequence of 7 words each composed of 8 bits. The first word represents information of the format of the related television signal (the currently-handled television signal). Specifically, the first word represents aspect ratio information (discrimination between an aspect ratio of 16:9 and an aspect ratio of 4:3), picture display format information (discrimination between a letter box and an ordinary format), track system information (discrimination among HD, NTSC, and EDTV), and telecine information (discrimination between the same frame or another). Here, "EDTV" is short for extended definition television. The second word has program ID information representing a program number. The third word represents information regarding the related audio signal (discrimination among "stereophonic", "monophonic", and "bilingual"). The third word also represents editing information (discrimination among editing start, editing end, and in-editing), corrective signal information (discrimination between the presence and the absence of a corrective signal), and control signal information (the duty ratios of control signals such as VISS and VASS). The fourth and fifth words represent text information containing character information according to a closed caption method. The sixth and seventh words are reserved.

The time code signal in the information signal IS has a sequence of 4 words each composed of 8 bits. The first word represents a frame number which is incremented every frame. The second, third, and fourth words represent "second", "minute", and "hour" respectively. It should be noted that the first word of the time code signal may represent a field number which is incremented every field. As shown in FIG. 4, a 1-frame HD signal has time segments corresponding to 1125 lines respectively. Here, "lines" are short for horizontal scanning lines. In FIG. 4, numerals such as "1119", "1125", "1", "41", "557", "604" denote line order numbers. The start of the first line coincides with the start of a vertical sync signal in an odd field of every frame.

An information signal IS is interposed in a time segment of an HD signal which corresponds to a given line or lines of every frame.

It is desirable that the line-corresponding signal segment or segments in which an information signal IS should be interposed are selected from among line-corresponding signal segments representative of display picture information with a low possibility of appearing on a display screen. Accordingly, in the case of an HD signal which is either a studio standard HD signal or a MUSE decoder output signal, it is preferable that an information signal IS is interposed in a signal time segment corresponding to a given line or lines

selected from among the 41-st line to the 66-th line, the 532-nd to the 557-th line, the 603-rd line to the 628-th line, and the 1095-th line to the 1120-th line. It is most preferable that an information signal IS is interposed in a signal time segment corresponding to a given line or lines selected from among the 41-st line, the 42-nd line, the 557-th line, the 603-rd line, the 604-th line, the 1119-th line, and the 1120-th line.

The 41-st line and the 603-rd line correspond to ineffective horizontal scanning lines in the case of a MUSE decoder output signal but correspond to effective horizontal scanning lines in the case of an HD signal in conformity to the studio standards. Accordingly, in the case where an HD signal is not encoded into a MUSE signal, it is preferable to place an information signal IS in a signal time segment corresponding to at least one of the 41-st line and the 603-rd line.

In the embodiment, the signal recording and reproducing apparatus converts an original HD signal into an information-signal-added HD signal by adding an information signal IS to a time segment of the original HD signal which corresponds to the 603-rd line. In addition, the signal recording and reproducing apparatus receives and accepts an HD signal containing an information signal IS at its time segment corresponding to the 603-rd line or the 604-th line.

In the case of an NTSC signal, it is preferable that an information signal IS is interposed in a signal time segment corresponding to the 19-th line.

Recording Side

A recording side (recording system) of the signal recording and reproducing apparatus operates in one of a W mode, a W-NT mode, and a 2NT mode. Operation of the recording side of the apparatus can be changed among the W mode, the W-NT mode, and the 2NT mode. During the W mode of operation, an HD signal is recorded on a magnetic tape driven at a standard speed. During the W-NT mode of operation, an NTSC signal representative of one program is recorded on a magnetic tape driven at a long-term-corresponding speed. During the 2NT mode of operation, NTSC signals representative of two programs are recorded on a magnetic tape driven at the standard speed.

The W mode of operation of the apparatus will now be described in detail. With reference to FIG. 5, the recording side of the signal recording and reproducing apparatus includes AGC sections 1, 2, and 3. An input Y signal (an input luminance signal) "aa" is fed to the AGC section 1 from a transmission line (not shown). Input PB and PR signals (input color signals) "bb" and "cc" are fed to the AGC sections 2 and 3 from the transmission line respectively. The input Y, PB, and PR signals "aa", "bb", and "cc" compose the video part of an HD signal or a MUSE decoder output signal.

The Y, PB, and PR signals are in conformity to the Japanese high-vision standards, and are generated from R, G, and B (red, green, and blue) signals by conversion expressed as follows.

$$Y=0.7154G+0.0721B+0.2125R$$

$$PB=0.5389(-0.7154G+0.9279B-0.2125R)$$

$$PR=0.6349(-0.7154G-0.0721B+0.7875R)$$

The AGC sections 1, 2, and 3 adjust the amplitude levels of the Y, PB, and PR signals in response to an output signal 4a from an A/D converter 4 which relates to the level reference signal in an information signal IS. The level reference signal contained in a signal segment corresponding to the 603-rd line is put in the first position of priority

regarding operation of the AGC sections 1, 2, and 3. In the case where a signal segment corresponding to the 603-rd line lacks the level reference signal but a signal segment corresponding to the 604-th line contains the level reference signal, the AGC sections 1, 2, and 3 use the level reference signal in the 604-th-line signal segment. In the case where neither a signal segment corresponding to the 603-rd line nor a signal segment corresponding to the 604-th line contains the level reference signal, the AGC sections 1, 2, and 3 use the amplitude level of a horizontal sync signal instead of the level reference signal in controlling the amplitude levels of the Y, PB, and PR signals. Even if the input Y, PB, and PR signals have excessively large amplitudes, the amplitude-level control by the AGC sections 1, 2, and 3 prevents the occurrence of errors in an information signal IS during signal processing by amplitude limiters 27 and 28 at later stages.

The resultant Y, PB, and PR signals "aa", "bb", and "cc", that is, the output signals of the AGC sections 1, 2, and 3, are fed to A/D converters 4, 5, and 6 respectively, and are converted into corresponding digital signals thereby. The digital Y, PB, and PR signals, that is, the output signals of the A/D converters 4, 5, and 6 are fed to a signal dividing section 7 before being separated into two groups thereby.

Operation of the signal dividing section 7 will now be described with reference to FIG. 6. In the case of an HD signal, some of 1125 lines composing one frame correspond to a vertical blanking period or other periods which have no relation with display picture information. Therefore, the recording of all 1125 lines into a recording medium causes a reduction of the efficiency of use of the recording medium regarding display picture information. To prevent such an efficiency reduction, as shown in FIG. 6, the Y, PB, and PR signals (composing the HD signal) are compressed into MUSE-corresponding signals by eliminating their segments related to sync components and related to regions above and below an effective display picture region. In the MUSE-corresponding signals, one frame is composed of 1032 lines equal in number to effective horizontal scanning lines of a frame of the MUSE format. Specifically, in the MUSE-corresponding signals, one frame is composed of the original 42-nd line to the original 557-th line, and the original 604-th line to the original 1119-th line. Further, the MUSE-corresponding signals are divided into line-corresponding segments which are separated into two groups as shown in the lower left and lower right sides of FIG. 6. The first group has signal segments related to the even-numbered lines while the second group has signal segments related to the odd-numbered lines. As a result, the Y signal is divided into a first sub Y signal 7a related to the even-numbered lines and a second sub Y signal 7d related to the odd-numbered lines. In addition, the PB signal is divided into a first sub PB signal 7b related to the even-numbered lines and a second sub PB signal 7e related to the odd-numbered lines. Furthermore, the PR signal is divided into a first sub PR signal 7c related to the even-numbered lines and a second sub PR signal 7f related to the odd-numbered lines.

The signal dividing section 7 includes, for example, frame memories and circuits for controlling the writing and reading of signals into and from the frame memories. In an alternative arrangement, the signal dividing section 7 includes switches changed in response to control signals having a period corresponding to one line.

The first Y, PB, and PR signals 7a, 7b, and 7c are fed from the signal dividing section 7 to a selector or switch 8. The second Y, PB, and PR signals 7d, 7e, and 7f are fed from the signal dividing section 7 to a selector or switch 9. The signal

processing by the signal dividing section 7 deletes signal segments corresponding to the 603-rd line or the 604-th line which contain the information signal IS. Accordingly, an information signal generator 20 (described later) produces a time-base-compressed TCI (time compressed integration) information signal 20a which is added to a record signal at a position corresponding to a given line.

The switch 8 receives third Y, PB, and PR signals 14a, 14b, and 14c from a signal converter 14. The switch 9 receives fourth Y, PB, and PR signals 15a, 15b, and 15c from a signal converter 15. The switches 8 and 9 select some of the first signals Y, PB, and PR signals 7a, 7b, and 7c, the second Y, PB, and PR signals 7d, 7e, and 7f, the third Y, PB, and PR signals 14a, 14b, and 14c, and the fourth Y, PB, and PR signals 15a, 15b, and 15c in response to a mode signal generated by a suitable device (not shown). When the mode signal represents the W mode, the switch 8 selects the first Y, PB, and PR signals 7a, 7b, and 7c and transmits the selected signals to a TCI converter 16 and the switch 9 selects the second Y, PB, and PR signals 7d, 7e, and 7f and transmits the selected signals to a TCI converter 17. When the mode signal represents the W-NT mode, the switch 8 selects the third Y, PB, and PR signals 14a, 14b, and 14c and transmits the selected signals to the TCI converter 16 and the switch 9 does not transmit any signals to the TCI converter 17. When the mode signal represents the 2NT mode, the switch 8 selects the third Y, PB, and PR signals 14a, 14b, and 14c and transmits the selected signals to the TCI converter 16 and the switch 9 selects the fourth Y, PB, and PR signals 15a, 15b, and 15c and transmits the selected signals to the TCI converter 17.

The TCI converter 16 combines the received PB and PR signals into line sequential color signals, and compresses the line sequential color signals into compressed line sequential color signals with respect to time base. The TCI converter 16 compresses the received Y signal into a compressed Y signal with respect to time base. Then, the TCI converter 16 multiplexes the compressed line sequential color signals and the compressed Y signal into a TCI signal 16a. The TCI converter 16 outputs the TCI signal 16a to a selector or switch 18.

The TCI converter 17 combines the received PB and PR signals into line sequential color signals, and compresses the line sequential color signals into compressed line sequential color signals with respect to time base. The TCI converter 17 compresses the received Y signal into a compressed Y signal with respect to time base. Then, the TCI converter 17 multiplexes the compressed line sequential color signals and the compressed Y signal into a TCI signal 17a. The TCI converter 17 outputs the TCI signal 17a to a selector or switch 19.

The switch 18 receives the TCI information signal 20a from the information signal generator 20. The switch 18 receives a corrective signal (calibration signal) 21a from a corrective signal generator (calibration signal generator) 21. The switch 18 receives a blanking signal 22a from a blanking signal generator 22. The blanking signal 22a contains a switching signal and a vertical sync signal.

The switch 18 multiplexes the TCI signal 16a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 18a. As shown in FIG. 7, during every period T1, the switch 18 selects the TCI signal 16a representing display picture information. During every period T2, the switch 18 selects the blanking signal 22a which contains the switching signal and the vertical sync signal. During every period T3, the switch 18 selects the TCI information signal 20a. During every period

T4, the switch 18 selects the corrective signal 21a. As shown in FIG. 7, a sequence of periods T2, T3, and T4 extends between a period T1 ending at picture information of the 1118-th line of a preceding frame and a period T1 starting from picture information of the 42-nd line of a present frame. In addition, a sequence of periods T2 and T4 extends between a period T1 ending at picture information of the 556-th line and a period T1 starting from picture information of the 604-th line. In FIG. 7, "SW" denotes a switching signal 22a for providing a margin during which the recording heads are switched or changed, and "V" denotes a vertical sync signal 22a. In addition, "DA" denotes the TCI information signal 20a, and "CAL" denotes the corrective signal (calibration signal) 21a.

The switch 19 receives the TCI information signal 20a from the information signal generator 20. The switch 19 receives the corrective signal (calibration signal) 21a from the corrective signal generator (calibration signal generator) 21. The switch 19 receives the blanking signal 22a from the blanking signal generator 22. The blanking signal 22a contains the switching signal and the vertical sync signal.

The switch 19 multiplexes the TCI signal 17a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 19a. As shown in FIG. 8, during every period T1, the switch 19 selects the TCI signal 17a representing display picture information. During every period T2, the switch 19 selects the blanking signal 22a which contains the switching signal and the vertical sync signal. During every period T3, the switch 19 selects the TCI information signal 20a. During every period T4, the switch 19 selects the corrective signal 21a. As shown in FIG. 8, a sequence of periods T2, T3, and T4 extends between a period T1 ending at picture information of the 1119-th line of a preceding frame and a period T1 starting from picture information of the 43-rd line of a present frame. In addition, a sequence of periods T2 and T4 extends between a period T1 ending at picture information of the 557-th line and a period T1 starting from picture information of the 605-th line. In FIG. 8, "SW" denotes a switching signal 22a for providing a margin during which the recording heads are switched or changed, and "V" denotes a vertical sync signal 22a. In addition, "DA" denotes the TCI information signal 20a, and "CAL" denotes the corrective signal (calibration signal) 21a.

The information signal generator 20 will now be described. As shown in FIG. 5, the information signal generator 20 includes a time code signal generator 200 containing counters for generating a time code signal 200a. As shown in FIG. 3, the time code signal 200a has 32 bits separated into four 8-bit words. The first word of the time code signal 200a is reset to "0" when an input HD signal starts to be recorded. The first word of the time code signal 200a is incremented by "1" in response to recording of every frame. The other words of the time code signal 200a contain information of "second", "minute", and "hour" which is generated in a suitable way. The time code signal 200a is fed to a divider 201 and an error correction signal generator 204.

The divider 201 serves to specify the relation between the type of the corrective signal (calibration signal) 21a and the time code signal 200a. The maximum number of different types of the corrective signal 21a is set to a predetermined natural number Q equal to 2 or more. The number of actually-used different types of the corrective signal 21a is set to a predetermined natural number R equal to or smaller than Q. In the embodiment, the number Q is equal to 5. The divider 201 divides the first word of the time code signal 200a (which represents the frame number) by the number Q

and generates a first control signal 201a representing the remainder of the division. Since the number Q is equal to 5, the first control signal 201a is changeable among states corresponding to "0", "1", "2", "3", and "4". The divider 201 outputs the first control signal 201a to a data signal generator 202 and a selector or switch 213 in the corrective signal generator (calibration signal generator) 21. The data signal generator 202 receives the first control signal 201a and the output signal 4a of the A/D converter 4. The data signal generator 202 extracts the information signal from the output signal 4a of the A/D converter 4. Specifically, the data signal generator 202 discriminates the information signal from other signals by using a given level (for example, a maximum level of a horizontal sync signal) as a threshold value. The data signal generator 202 subjects the information signal to error detection and correction. The data signal generator 202 changes the data signal in the information signal into a new data signal 202a by updating the program ID information, the editing information, the corrective signal information, and others therein. The data signal generator 202 outputs the new data signal 202a to the error signal generator 204. An audio identification (discrimination) signal "vv" is contained in the data signal 202a. The data signal generator 202 receives the audio identification signal "vv" from a suitable device (not shown). The corrective signal information is used in discrimination between the presence and the absence of a corrective signal (calibration signal). Three different types of the corrective signal are prepared in the corrective signal generator 21. The first type, the second type, and the third type of the corrective signal are selected in the corrective signal generator 21 when the first control signal 201a assumes states of "0", "1", and "2" respectively. The corrective signal is not recorded when the first control signal 201a assumes one of states of "3" and "4". Accordingly, the data signal generator 202 sets the corrective signal information to "1" when the first control signal 201a assumes one states of "0", "1", and "2". In addition, the data signal generator 202 sets the corrective signal information to "0" when the first control signal 201a assumes one of states of "3" and "4". In the absence of an information signal from the signal segments corresponding to the 603-rd line and the 604-th line (for example, in the case where an input HD signal agrees with a broadcasting HD signal), the data signal generator 202 produces a data signal 202a in response to the output signal of a discrimination circuit (not shown) for discriminating information, such as information of the type of the video signal and the type of the audio signal, which is necessary in data signal generation.

The error correction signal generator 204 receives the time code signal 200a and the data signal 202a, and generates words of a Reed-Solomon code (an error correction signal) in response to the signals 200a and 202a. The error correction signal generator 204 adds the generated code words (the error correction signal) to the time code signal 200a and the data signal 202a. The error correction signal generator 204 outputs the addition-resultant signal to a modulator 206.

An added-signal generator 205 produces a preamble signal and a sync signal, and outputs the preamble signal and the sync signal to the modulator 206.

The output signal of the error correction signal generator 204 and the output signal of the added-signal generator 205, which are received by the modulator 206, agree with 2-value signals changeable between two levels corresponding to "0" and "1" in time domain. The modulator 206 converts the received 2-value signals into 3-value signals while combining the received 2-value signals. This conversion is to

prevent the levels of the related signals from exceeding limiter levels in limiters 27 and 28. Specifically, the modulator 206 uses a clock signal having a waveform such as shown in the portion (A) of FIG. 9. A sum of six periods of the clock signal corresponds to one bit of a received signal (the output signal of the error correction signal generator 204 or the added-signal generator 205) which has a waveform such as shown in the portion (B) of FIG. 9. The level of the received signal is changeable between 20 IRE and 80 IRE corresponding to logic states of "0" and "1" respectively. The modulator 206 executes the following modulation process. In the case of the "0" state of the received signal which is preceded by the "1" state, that is, in the case where the received signal has just changed from "1" to "0", the level of the modulation-resultant signal changes as 50 IRE, 20 IRE, 20 IRE, 20 IRE, 20 IRE, and 20 IRE at respective sample moments in six periods of the clock signal as shown in the portion (C) of FIG. 9. In the case of the "1" state of the received signal which is preceded by the "0" state, that is, in the case where the received signal has just changed from "0" to "1", the level of the modulation-resultant signal changes as 50 IRE, 80 IRE, 80 IRE, 80 IRE, 80 IRE, and 80 IRE at respective sample moments in six periods of the clock signal as shown in the portion (C) of FIG. 9. In the case of the "1" state of the received signal which is preceded by the "1" state, that is, in the case where the received signal has remained "1" during two bits, the level of the modulation-resultant signal keeps unchanged as 80 IRE, 80 IRE, 80 IRE, 80 IRE, 80 IRE, and 80 IRE at respective sample moments in six periods of the clock signal. In the case of the "0" state of the received signal which is preceded by the "0" state, that is, in the case where the received signal has remained "0" during two bits, the level of the modulation-resultant signal keeps unchanged as 20 IRE, 20 IRE, 20 IRE, 20 IRE, 20 IRE, and 20 IRE at respective sample moments in six periods of the clock signal. Thus, an intermediate level of 50 IRE is inserted in a level change of the received signal between 20 IRE and 80 IRE. The insertion of the intermediate level of 50 IRE reduces a rate of a level change of the modulation-resultant signal so that the level of the related output signal of an emphasis section 25 or 26 can be prevented from exceeding a limiter level in the limiter 27 or 28 as shown in the portion (D) of FIG. 9. The respective values of the 3-value signal correspond to 20 IRE, 50 IRE, and 80 IRE. The modulator 206 outputs the modulation-resultant signal to a switch or selector 207.

The emphasis sections 25 and 26 emphasize high-frequency signal components, and hence cause greater spike levels at time positions corresponding to display picture portions immediately after edges in a display picture. The conversion of the 2-value signal into the 3-value signal by the modulator 206 suppresses such spike levels, thereby preventing the loss of edge information which would occur when the signal level exceeds the limiter level in the limiter 27 or 28.

A level reference signal generator 203 produces a level reference signal with a predetermined normal reference level (50 IRE). The level reference signal is outputted from the generator 203 to the switch 207. A sync signal generator (not shown) produces a sync signal which is fed to the switch 207.

The switch 207 time-division-multiplexes the output signal of the modulator 206, the level reference signal, and the sync signal into a TCI information signal 20a which has a waveform such as shown in FIG. 10. The information signal interposed in the 603-rd or 604-th line segment of the Y

signal "aa" is time-base-compressed into a segment of the TCI information signal 20a which occupies a period T1 in FIG. 10. The rate of compression of the information signal is set equal to the rate of compression of the Y signal "aa".

Information signal may be interposed in at least one of the PB signal "bb" and the PR signal "cc".

The corrective signal generator (calibration signal generator) 21 will now be described. As shown in FIG. 5, the corrective signal generator 21 includes ROM's 210, 211, and 212 storing first, second, and third predetermined corrective signals (first, second, and third predetermined calibration signals) 210a, 211a, and 212a respectively. The first, second, and third corrective signals 210a, 211a, and 212a agree with the first type, the second type, and the third type of the corrective signal 21a respectively. The corrective signal generator 21 also includes a switch or selector 213 receiving the corrective signals 210a, 211a, and 212a from the ROM's 210, 211, and 212. The switch 213 receives a sync signal and a blanking signal from ROM's (not shown). The blanking signal has a pedestal level. As previously described, the switch 213 receives the first control signal 201a from the divider 201 in the information signal generator 20. The switch 213 selects one or more of the corrective signals 210a, 211a, and 212a, the sync signal, and the blanking signal in response to the first control signal 201a, and transmits the selected signal or signals to the switches 18 and 19. Specifically, the switch 213 selects the first corrective signal 210a when the first control signal 201a assumes "0". The switch 213 selects the second corrective signal 211a when the first control signal 201a assumes "1". The switch 213 selects the third corrective signal 212a when the first control signal 201a assumes "2". The switch 213 selects the sync signal and the blanking signal when the first control signal 201a assumes "3" and "4". Accordingly, the first control signal 201a determines and thus indicates the type of the currently-selected corrective signal. The corrective signals 210a, 211a, and 212a contain ramp signals for calibrating the linearities between the even-line processing system and the odd-line processing system, gray scale signals for adjusting the direct-current levels and the amplitude levels between the two systems, multi-burst signals for calibrating the frequency characteristics between the two systems, and 2T pulse signals for calibrating the phase characteristics between the two systems. For example, the 2T pulse signals have a sine-square form and a half width which equals a period of a frequency corresponding to a half of the related band.

The blanking signal generator 22 includes ROM's storing data representing the blanking signal 22a. The blanking signal generator 22 produces the blanking signal 22a which contains the switching signal and the vertical sync signal. The blanking signal generator 22 outputs the blanking signal 22a to the switches 18 and 19. As previously described, the blanking signal 22a which contains the switching signal "SW" and the vertical sync signal "V" is inserted during the periods T2 in FIGS. 7 and 8.

As previously described, the switch 18 multiplexes the TCI signal 16a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 18a. The switch 18 outputs the composite signal 18a to a D/A converter 23. The composite signal 18a is changed into a corresponding analog signal by the D/A converter 23.

As previously described, the switch 19 multiplexes the TCI signal 17a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 19a. The switch 19 outputs the composite signal 19a to a D/A converter 24. The composite signal 19a is changed into a corresponding analog signal by the D/A converter 24.

The emphasis sections 25 and 26 receive the output signals of the D/A converters 23 and 24 respectively. The emphasis sections and 26 emphasize high-frequency components of the received signals in a horizontal direction, and output the emphasis-resultant signals to the limiters 27 and 28 respectively. The devices 27 and 28 limit the amplitudes of the emphasis-resultant signals with respect to predetermined limiter levels. FM modulators 29 and 30 receive the output signals of the limiters 27 and 28, and subject the received signals to frequency modulation of a given deviation respectively. The output signal of the FM modulator 29 is fed via a recording amplifier (not shown) to magnetic heads (video heads) 1A and 1B before being recorded on a magnetic tape TT thereby. The output signal of the FM modulator 30 is fed via a recording amplifier (not shown) to magnetic heads (video heads) 2A and 2B before being recorded on the magnetic tape TT thereby. The magnetic heads 1A, 1B, 2A, and 2B are mounted on a rotary drum.

The signal record pattern on the magnetic tape TT will now be described with reference to FIGS. 11 and 12, in which the numerals denote the line order numbers; "SW" denotes a switching signal; "V" denotes a vertical sync signal; "CAL" denotes a corrective signal (calibration signal); and "DA" denotes a TCI information signal. As shown in FIGS. 11 and 12, the magnetic tape TT is provided with video and audio tracks for storing video information, audio information, and other information, and the video and audio tracks extend in directions oblique with respect to the magnetic tape.

With reference to FIG. 11, during the W mode of operation of the apparatus, the output signal of the FM modulator 29 which relates to the even-numbered lines is recorded on a video track between "SW" and "556(1/2)" via the magnetic head 1A, and is recorded on a video track between "556(1/2)" and "1118" via the magnetic head 1B. On the other hand, the output signal of the FM modulator 30 which relates to the odd-numbered lines is recorded on a video track between "SW" and "557(1/2)" via the magnetic head 2A, and is recorded on a video track between "557(1/2)" and "1119" via the magnetic head 2B. Two adjacent magnetic heads of the magnetic heads 1A, 1B, 2A, and 2B can simultaneously execute recording processes. As will be described later, magnetic heads (audio heads) 3A and 3B preceding the video heads 1A, 1B, 2A, and 2B form audio tracks "A" and "B" respectively.

The attachment heights of the magnetic heads 1A, 1B, 2A, 2B, 3A, and 3B may be modified so as to provide another signal record pattern on the magnetic tape TT which is shown in FIG. 12.

As previously described, during the W-NT mode of operation of the apparatus, an NTSC signal representative of one program is recorded on a magnetic tape driven at a long-term-corresponding speed. During the 2NT mode of operation of the apparatus, NTSC signals representative of two programs are recorded on a magnetic tape driven at the standard speed.

The W-NT mode of operation and the 2NT mode of operation will now be described in more detail. During the W-NT mode of operation, the tape running speed is set to one third of the standard tape running speed, and an NTSC signal is subjected to given processing and then 1-field segments of the resultant NTSC signal are recorded on respective tracks on the magnetic tape. During the 2NT mode of operation, the tape running speed is set to the standard tape running speed, and NTSC signals of two programs are subjected to given processing and then 1-field segments of the resultant NTSC signals are recorded on

respective video tracks shown in FIGS. 11 and 12. With reference to FIG. 5, the recording section of the signal recording and reproducing apparatus includes AGC sections 10 and 11. A first NTSC signal "dd" is fed to the AGC section 10 from a transmission line (not shown). A second NTSC signal "ee" is fed to the AGC section 11 from a transmission line (not shown). The AGC sections 10 and 11 adjust the amplitude levels of the NTSC signals "dd" and "ee" in response to output signals 12a and 13a from A/D converters 12 and 13 which relates to the level reference signals in information signals IS. The adjustment-resultant NTSC signals "dd" and "ee", that is, the output signals of the AGC sections 10 and 11, are fed to the A/D converters 12 and 13 respectively, and are converted into corresponding digital signals thereby. The digital NTSC signals, that is, the output signals 12a and 13a of the A/D converters 12 and 13, are fed to signal converters 14 and 15 respectively. The signal converter 14 changes the output signal 12a of the A/D converter 12 into third Y, PB, and PR signals 14a, 14b, and 14c through given signal processing. The signal converter 14 outputs the third Y, PB, and PR signals 14a, 14b, and 14c to the switch 8. The signal converter 15 changes the output signal 13a of the A/D converter 13 into fourth Y, PB, and PR signals 15a, 15b, and 15c through given signal processing. The signal converter 15 outputs the fourth Y, PB, and PR signals 15a, 15b, and 15c to the switch 9.

It should be noted that the AGC section 11, the A/D converter 13, and the signal converter 15 which relate to the second NTSC signal "ee" are active during the 2NT mode of operation but are inactive during the W-NT mode of operation. On the other hand, the AGC section 10, the A/D converter 12, and the signal converter 14 which relate to the first NTSC signal "dd" are active during both the 2NT mode of operation and the W-NT mode of operation.

The switch 8 selects the third Y, PB, and PR signals 14a, 14b, and 14c, and transmits the selected signals to the TCI converter 16.

The switch 9 selects the fourth Y, PB, and PR signals 15a, 15b, and 15c, and transmits the selected signals to the TCI converter 17.

The TCI converter 16 compresses the third PB and PR signals 14b and 14c into compressed PB and PR signals with respect to time base. In addition, the TCI converter 16 compresses the third Y signal 14a into a compressed Y signal with respect to time base.

Then, the TCI converter 16 multiplexes the compressed Y, PB, and PR signals into a TCI signal 16a. The TCI converter 16 outputs the TCI signal 16a to the switch 18.

The TCI converter 17 compresses the fourth PB and PR signals 15b and 15c into compressed PB and PR signals with respect to time base. In addition, the TCI converter 17 compresses the fourth Y signal 15a into a compressed Y signal with respect to time base. Then, the TCI converter 17 multiplexes the compressed Y, PB, and PR signals into a TCI signal 17a. The TCI converter 17 outputs the TCI signal 17a to the switch 19.

The switch 18 multiplexes the TCI signal 16a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 18a having a waveform such as shown in FIGS. 13 and 14. It should be noted that, in these drawings, "SW" denotes a switching signal 22a for providing a margin during which the recording heads are switched or changed, and "V" denotes a vertical sync signal 22a. In addition, "DA" denotes the TCI information signal 20a, and "CAL" denotes the corrective signal (calibration signal) 21a. As shown in FIG. 13, the switch 18 replaces the portion of the TCI signal 16a, which

corresponds to the 3-rd line to the 7-th line, by a sequence of two switching signals "SW", a vertical sync signal "V", a TCI information signal "DA", and a corrective signal "CAL". As shown in FIG. 14, the switch 18 replaces the portion of the TCI signal 16a, which corresponds to the 265-th line to the 269-th line, by a sequence of two switching signals "SW", two vertical sync signals "V", and a corrective signal "CAL". The switch 18 selects and passes the other portions of the TCI signal 16a.

The switch 19 multiplexes the TCI signal 17a, the TCI information signal 20a, the corrective signal 21a, and the blanking signal 22a into a composite signal 19a having a waveform such as shown in FIGS. 13 and 14. Operation of the switch 19 is similar to operation of the switch 18, and thus description thereof will be omitted.

The composite signal 18a is transmitted from the switch 18 to the magnetic heads 1A and 1B via the devices 23, 25, 27, and 29 before being recorded on the magnetic tape TT thereby. The composite signal 19a is transmitted from the switch 19 to the magnetic heads 2A and 2B via the devices 24, 26, 28, and 30 before being recorded on the magnetic tape TT thereby.

FIG. 15 shows the signal record pattern of the magnetic tape TT which occurs during the 2NT mode of operation. FIG. 16 shows the signal record pattern of the magnetic tape TT which occurs during the W-NT mode of operation. In FIGS. 15 and 16: the numerals denote the line order numbers; "SW" denotes a switching signal; "V" denotes a vertical sync signal; "CAL" denotes a corrective signal (calibration signal); and "DA" denotes a TCI information signal.

The recording of an audio signal will now be described.

During the W mode of operation of the apparatus, an information signal in an input HD signal contains audio identification information representing the type of a related audio signal (the stereophonic type, the monophonic type, or the bilingual type). The information signal is separated from the output signal 4a of the A/D converter 4, and is then fed to the information signal generator 20. As previously described, the information signal generator 20 places the information signal in the TCI information signal 20a. Then, the TCI information signal 20a is processed by the devices 18, 19, 23, 24, 25, 26, 27, 28, 29, and 30 before being recorded via the magnetic heads 1A, 1B, 2A, and 2B on the magnetic tape TT as a signal "DA" in FIG. 11.

With reference to FIG. 5, an input audio signal "ww" of the right channel is fed to an audio signal recording processor 80. In addition, an input audio signal "xx" of the left channel is fed to an audio signal recording processor 81. Each of the audio signal recording processors 80 and 81 includes an amplifier (not shown) acting on the input audio signal, a noise reduction circuit (not shown) acting on the output signal of the amplifier, and a preemphasis circuit (not shown) which emphasizes high-frequency components of the output signal of the noise reduction circuit. The output signal of the audio signal recording processor 80, that is, the output signal of the preemphasis circuit therein, is fed to an FM modulator 82, and is converted thereby into an FM audio signal having a central frequency of 1.7 MHz and a frequency deviation of ± 150 kHz. The output signal of the audio signal recording processor 81, that is, the output signal of the preemphasis circuit therein, is fed to an FM modulator 83, and is converted thereby into an FM audio signal having a central frequency of 1.3 MHz and a frequency deviation of ± 150 kHz. The FM audio signals are transmitted from the FM modulators 82 and 83 to an adder 84 via level adjusters (not shown), being combined by the adder 84 into a multi-

plexed FM audio signal. During the W mode of operation of the apparatus, the multiplexed FM audio signal is fed from the adder 84 to the magnetic heads 3A and 3B, and is recorded thereby on audio tracks "A" and "B" on the magnetic tape TT in FIG. 11.

In the case of a broadcasting MUSE signal, a MUSE decoder (not shown) separates the MUSE signal into input Y, PB, and PR signals "aa", "bb", and "cc" and an audio identification signal "vv".

The audio identification signal "vv" is generated from information interposed in a segment of the MUSE signal which corresponds to a given line of every frame. The input Y, PB, and PR signals "aa", "bb", and "cc" and the audio identification signal "vv" are fed to the signal recording and reproducing apparatus.

During the W-NT mode of operation of the apparatus, an NTSC signal "dd" is fed to the AGC section 10, and simultaneously audio identification information in the output signal 12a of the A/D converter 12 is fed to the data signal generator 202 in the information signal generator 20. In addition, input audio signals "ww" and "xx" of the right and left channels are fed to the audio signal recording processors 80 and 81 respectively.

During the W-NT mode of operation of the apparatus, the tape running speed is set to one third of the standard tape running speed, and the NTSC signal is subjected to given processing and then 1-field segments of the resultant NTSC signal are recorded on respective tracks on the magnetic tape TT as shown in FIG. 16. The information signal generator 20 places the audio identification information in the TCI information signal 20a. Then, the TCI information signal 20a is processed by the devices 18, 23, 25, 27, and 29 before being recorded via the magnetic heads 1A and 1B on the magnetic tape TT as a signal "DA" in FIG. 16. On the other hand, the input audio signals "ww" and "a" are processed by the audio signal recording processors 80 and 81 respectively. The output signals of the audio signal recording processors 80 and 81 are converted by the FM modulators 82 and 83 into FM audio signals having central frequencies of 1.7 MHz and 1.3 MHz and a frequency deviation of ± 150 kHz. The FM audio signals are combined by the adder 84 into a multiplexed FM audio signal. During the W-NT mode of operation of the apparatus, the multiplexed FM audio signal is recorded by the magnetic heads 3A and 3B into deep layer portions of the magnetic tape TT.

During the 2NT mode of operation of the apparatus, first and second NTSC signals "dd" and "ee" are fed to the AGC sections 10 and 11 respectively, and simultaneously audio identification information in the output signals 12a and 13a of the A/D converters 12 and 13 is fed to the data signal generator 202 in the information signal generator 20. In addition, input audio signals "ww" and "xx" of the right and left channels are fed to the audio signal recording processors 80 and 81 respectively.

During the 2NT mode of operation of the apparatus, the tape running speed is set to the standard tape running speed, and the NTSC signals are subjected to given processing and then 1-field segments of the resultant NTSC signals are recorded on respective video tracks on the magnetic tape TT as shown in FIG. 11. The information signal generator 20 places the audio identification information in the TCI information signal 20a. Then, the TCI information signal 20a is processed by the devices 18, 19, 23, 24, 25, 26, 27, 28, 29, and 30 before being recorded via the magnetic heads 1A, 1B, 2A, and 2B on the magnetic tape IT as a signal "DA" in FIG. 15. On the other hand, the input audio signals "ww" and "xx" related to the first program (the first NTSC signal "dd")

are processed by the audio signal recording processors 80 and 81 respectively. The output signals of the audio signal recording processors 80 and 81 are converted by the FM modulators 82 and 83 into FM audio signals having central frequencies of 1.7 MHz and 1.3 MHz and a frequency deviation of ± 150 kHz. The input audio signals "ww" and "xx" related to the second program (the second NTSC signal "ee") are processed by audio signal recording processors (not shown) respectively. The output signals of the audio signal recording processors are converted by FM modulators (not shown) into FM audio signals having central frequencies of 2.7 MHz and 2.3 MHz and a frequency deviation of ± 150 kHz. The FM audio signals related to the first program and the FM audio signals related to the second program are combined by the adder 84 into a multiplexed FM audio signal. During the 2NT mode of operation of the apparatus, the multiplexed FM audio signal is recorded by the magnetic heads 3A and 3B on audio tracks of the magnetic tape TT.

The audio identification signal "vv" and the input audio signals "ww" and "xx" are fed to the signal recording and reproducing apparatus while the input NTSC signal or signals are fed thereto. In Japanese ground-wave TV broadcasting, a sub carrier AM-modulated with an audio mode signal is multiplexed with a main carrier for frequency modulation of an audio signal, and the resultant audio signal and an NTSC signal are combined into a television signal. The sub carrier is separate from the main carrier by a frequency of about 55 kHz. The audio mode signal is either a stereophonic audio mode signal with a frequency of 982.5 Hz or a bilingual audio mode signal with a frequency of 922.5 Hz. The absence of the stereophonic audio mode signal and the bilingual audio mode signal indicates that the related audio signal is of the monophonic type.

During the W-NT mode of operation of the apparatus, a tuner (not shown) divides a received television signal into an NTSC signal "dd", input audio signals "ww" and "xx", and an audio identification signal "vv". The audio identification signal "vv" is derived from the audio mode signal in the received television signal. The NTSC signal "dd", the input audio signals "ww" and "xx", and the audio identification signal "vv" are fed to the apparatus via transmission lines (not shown).

During the 2NT mode of operation of the apparatus, a first tuner (not shown) divides a first received television signal (a first program) into a first NTSC signal "dd", input audio signals "ww" and "xx", and an audio identification signal "vv". The audio identification signal "vv" is derived from the audio mode signal in the received television signal. The first NTSC signal "dd", the input audio signals "ww" and "xx", and the audio identification signal "vv" are fed to the apparatus via transmission lines (not shown). At the same time, a second tuner (not shown) divides a second received television signal (a second program) into a second NTSC signal "ee", input audio signals "ww" and "xx", and an audio identification signal "vv". The audio identification signal "vv" is derived from the audio mode signal in the received television signal. The second NTSC signal "ee", the input audio signals "ww" and "xx", and the audio identification signal "vv" are fed to the apparatus via transmission lines (not shown).

Reproducing Side

A reproducing side (reproducing system) of the signal recording and reproducing apparatus operates in one of the W mode, the W-NT mode, and the 2NT mode. Operation of the reproducing side of the apparatus can be changed among the W mode, the W-NT mode, and the 2NT mode.

The W mode of operation of the apparatus will now be described in detail. With reference to FIG. 17, the reproducing side of the signal recording and reproducing apparatus includes an FM demodulator 40 following the magnetic heads 1A and 1B, and an FM demodulator 41 following the magnetic heads 2A and 2B. Signals are reproduced from the magnetic tape TT by the magnetic heads 1A, 1B, 2A, and 2B. The reproduced signals are fed via amplifiers (not shown) to the FM demodulators 40 and 41, being subjected to FM demodulation thereby. The demodulation-resultant signals, that is, the output signals of the FM demodulators 40 and 41, are fed to deemphasis sections 42 and 43 having functions inverse with respect to the functions of the emphasis sections 25 and 26 in the recording side of the apparatus. Specifically, the deemphasis sections 42 and 43 attenuate high-frequency components of the output signals of the FM demodulators 40 and 41 in a horizontal direction. The output signals of the deemphasis sections 42 and 43 are fed to A/D converters 44 and 45, being converted thereby into corresponding digital reproduced signals 44a and 45a. The A/D converters 44 and 45 outputs the digital reproduced signals 44a and 45a to correcting sections 46 and 47 respectively.

The correcting section 46 calibrates or corrects the reproduced signal 44a in response to a control signal 48a representing the type of the previously-indicated corrective signal (calibration signal) 21a. The control signal 48a will be described later. The correcting section 47 calibrates or corrects the reproduced signal 45a in response to a control signal 49a representing the type of the previously-indicated corrective signal (calibration signal) 21a. The control signal 49a will be described later. The reproducing section of the apparatus has a correcting structure which can deal with at least some of all the types of the corrective signals.

According to an example of correction responsive to the first-type, the second-type, and the third-type corrective signals 210a, 211a, and 212a, the control signals 48a and 49a are fed to the corrective signal generator 21 in place of the first control signal 201a so that the corrective signal generator 21 produces and outputs an original corrective signal which corresponds to the currently-reproduced corrective signal. The original corrective signal and the corresponding reproduced corrective signal are compared in level by a comparator in the correcting section 46 or 47 to derive a difference therebetween, and the reproduced signal 44a or 45a is corrected in response to the resultant difference so that the corresponding reproduced corrective signal will be essentially equal to the original corrective signal in later frames. It should be noted that the types of the corrective signals generated by the recording side of the apparatus may be equal to or different from the types of the corrective signals used by the reproducing side of the apparatus.

The output signal of the correcting section 46 is fed to a TCI discriminator (TCI detector) 50 and a TCI inverse converter 56. The output signal of the correcting section 47 is fed to a TCI discriminator (TCI detector) 51 and a TCI inverse converter 57.

The TCI discriminator 50 extracts a TCI information signal 20a from the output signal of the correcting section 46. The TCI discriminator 50 samples and holds the level of the TCI information signal 20a which occurs during a period t2 or t3 in FIG. 10. The TCI discriminator 50 discriminates "0" and "1" in bits of the TCI information signal 20a while using the sampled and held level as a threshold value. The TCI discriminator 50 derives level information from a level reference signal in the TCI information signal 20a. The output signal 50a of the TCI discriminator 50 is fed to a correction controller 48 and a signal generator 52.

The TCI discriminator 51 extracts a TCI information signal 20a from the output signal of the correcting section 47. The TCI discriminator 51 samples and holds the level of the TCI information signal 20a which occurs during a period t2 or t3 in FIG. 10. The TCI discriminator 51 discriminates "0" and "1" in bits of the TCI information signal 20a while using the sampled and held level as a threshold value. The TCI discriminator 51 derives level information from a level reference signal in the TCI information signal 20a. The output signal 51a of the TCI discriminator 51 is fed to a correction controller 49 and a signal generator 53.

The correction controller 48 generates the control signal 48a in response to the output signal 50a of the TCI discriminator 50. The control signal 48a corresponds to the control signal 201a in the recording side of the apparatus, and indicates the type of the currently-reproduced corrective signal. The correction controller 48 includes a divider 480, an error detector 481, a corrective signal information detector 482, and a switch or selector 483. The divider 480 receives the output signal 50a of the TCI discriminator 50. Similarly to the operation of the divider 201 in the recording side of the apparatus, the divider 480 divides the first word of the time code signal 200a (which represents the frame number) in the signal 50a by the number Q (Q=5), and generates a primary control signal representing the remainder of the division. The divider 480 outputs the primary control signal to the switch 483. The error detector 481 receives the output signal 50a of the TCI discriminator 50. The error detector 481 decides whether the information signal in the signal 50a is accurate or wrong by referring to the error correction signal therein. When the information signal is decided to be wrong, the error detector 481 outputs a "0" signal to the switch 483. When the information signal is decided to be accurate, the error detector 481 outputs a "1" signal to the switch 483. The corrective signal information detector 482 receives the output signal 50a of the TCI discriminator 50. The corrective signal information detector 482 extracts the corrective signal information from the information signal in the signal 50a. When the corrective signal information indicates the absence of a corrective signal, the corrective signal information detector 482 outputs a "0" signal to the switch 483. When the corrective signal information indicates the presence of a corrective signal, the corrective signal information detector 482 outputs a "1" signal to the switch 483. In the case where both the output signals of the error detector 481 and the corrective signal information detector 482 are "1", the switch 483 passes the primary control signal to the correcting section 46 as the control signal 48a. In other cases, the switch 483 inhibits the transmission of the primary control signal to the correcting section 46. The correction controller 49 generates the control signal 49a in response to the output signal 51a of the TCI discriminator 51. The structure and operation of the correction controller 49 are similar to those of the correction controller 48.

The signal generator 52 expands the output signal 50a of the TCI discriminator 50 with respect to time base, and recovers the information signal therefrom. The TCI signal generator 52 outputs the recovered information signal to a switch or selector 63. The switch 63 interposes the information signal in a time segment of a Y signal which relates to the 603-rd line of every frame. The TCI inverse converters 56 and 57 have functions inverse with respect to the functions of the TCI converters 16 and 17 in the recording side of the apparatus. As previously described, the TCI inverse converter 56 receives the output signal of the correcting section 46 which contains the compressed line sequential

color signals and the compressed luminance signal. The TCI inverse converter 56 expands the compressed line sequential color signals and the compressed luminance signal with respect to time base, and thereby returns them into the original line sequential color signals and the original luminance signal (the reproduced Y signal) 56a. The TCI converter 56 demodulates the original line sequential color signals into the reproduced PB and PR signals 56b and 56c. The TCI converter 56 outputs the reproduced Y, PB, and PR signals 56a, 56b, and 56c to a signal combining section 62 via a switch or selector 58. The reproduced Y, PB, and PR signals 56a, 56b, and 56c relate to the even-numbered lines of every frame.

As previously described, the TCI inverse converter 57 receives the output signal of the correcting section 47 which contains the compressed line sequential color signals and the compressed luminance signal. The TCI inverse converter 57 expands the compressed line sequential color signals and the compressed luminance signal with respect to time base, and thereby returns them into the original line sequential color signals and the original luminance signal (the reproduced Y signal) 57a. The TCI converter 57 demodulates the original line sequential color signals into the reproduced PB and PR signals 57b and 57c. The TCI converter 57 outputs the reproduced Y, PB, and PR signals 57a, 57b, and 57c to the signal combining section 62 via a switch or selector 59. The reproduced Y, PB, and PR signals 57a, 57b, and 57c relate to the odd-numbered lines of every frame.

The signal combining section 62 has a function inverse with respect to the function of the signal dividing section 7 in the recording side of the apparatus. The signal combining section 62 combines a set of the Y, PB, and PR signals 56a, 56b, and 56c and a set of the Y, PB, and PR signals 57a, 57b, and 57c into a set of the composite Y, PB, and PR signals. Specifically, the Y signal 56a and the Y signal 57a are combined into the composite Y signal. The PB signal 56b and the PB signal 57b are combined into the composite PB signal. The PR signal 56c and the PR signal 57c are combined into the composite PR signal.

The signal combining section 62 outputs the composite Y signal to the switch 63 by which the information signal is added to the 603-rd line segment of the composite Y signal. The switch 63 outputs the resultant Y signal to a D/A converter 64. The resultant Y signal is converted by the D/A converter 64 into an analog Y signal "ff". The D/A converter 64 outputs the analog Y signal "ff" to a transmission line (not shown). The signal combining section 62 outputs the composite PB signal to a D/A converter 65. The composite PB signal is converted by the D/A converter 65 into an analog PB signal "gg". The D/A converter 65 outputs the analog PB signal "gg" to a transmission line (not shown). The signal combining section 62 outputs the composite PR signal to a D/A converter 66. The composite PR signal is converted by the D/A converter 66 into an analog PR signal "hh". The D/A converter 66 outputs the analog PR signal "hh" to a transmission line (not shown).

The W-NT mode of operation of the apparatus will now be described. During the W-NT mode of operation, only apparatus portions related to the magnetic heads 1A and 1B are active, and an NTSC signal of one program is reproduced from the magnetic tape TT which is driven at the long-term-corresponding speed. The devices 1A, 1B, 40, 42, 44, 46, 48, 50, and 52 operate similarly to the operations thereof which occur during the W mode of operation of the apparatus.

During the W-NT mode of operation, the TCI inverse converter 56 receives the output signal of the correcting

section 46 which contains the compressed Y, PB, and PR signals. The TCI inverse converter 56 expands the compressed Y, PB, and PR signals with respect to time base, and thereby returns them into the original Y, PB, and PR signals (the reproduced Y, PB, and PR signals). The TCI converter 56 outputs the reproduced Y, PB, and PR signals to an inverse signal converter 60 via the switch 58. The inverse signal converter 60 has a function inverse with respect to the function of the signal converter 14 in the recording side of the apparatus. The inverse signal converter 60 combines the reproduced Y, PB, and PR signals into a composite NTSC signal. The inverse signal converter 60 outputs the composite NTSC signal to a switch or selector 54. In addition, the TCI signal generator 52 outputs the recovered information signal to the switch 54. The switch 54 interposes the information signal in a time segment of the composite NTSC signal which relates to the 19-th line of every frame. The switch 54 outputs the resultant composite NTSC signal to a D/A converter 67. The resultant composite NTSC signal is converted by the D/A converter 67 into an analog NTSC signal "ii". The D/A converter 67 outputs the analog NTSC signal "ii" to a transmission line (not shown).

The 2NT mode of operation of the apparatus will now be described. During the 2NT mode of operation, NTSC signals of two programs are reproduced from the magnetic tape TT which is driven at the standard speed. The devices 1A, 1B, 2A, 2B, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, and 53 operate similarly to the operations thereof which occur during the W mode of operation of the apparatus.

During the 2NT mode of operation, the TCI inverse converter 56 receives the output signal of the correcting section 46 which contains the first compressed Y, PB, and PR signals. The TCI inverse converter 56 expands the first compressed Y, PB, and PR signals with respect to time base, and thereby returns them into the first original Y, PB, and PR signals (the first reproduced Y, PB, and PR signals). The TCI converter 56 outputs the first reproduced Y, PB, and PR signals to the inverse signal converter 60 via the switch 58. The inverse signal converter 60 combines the first reproduced Y, PB, and PR signals into a first composite NTSC signal. The inverse signal converter 60 outputs the first composite NTSC signal to the switch 54. In addition, the TCI signal generator 52 outputs the recovered information signal to the switch 54. The switch 54 interposes the information signal in a time segment of the first composite NTSC signal which relates to the 19-th line of every frame. The switch 54 outputs the resultant first composite NTSC signal to the D/A converter 67. The resultant first composite NTSC signal is converted by the D/A converter 67 into a first analog NTSC signal "ii". The D/A converter 67 outputs the first analog NTSC signal "ii" to the transmission line (not shown).

During the 2NT mode of operation, the TCI inverse converter 57 receives the output signal of the correcting section 47 which contains the second compressed Y, PB, and PR signals. The TCI inverse converter 57 expands the second compressed Y, PB, and PR signals with respect to time base, and thereby returns them into the second original Y, PB, and PR signals (the second reproduced Y, PB, and PR signals). The TCI converter 57 outputs the second reproduced Y, PB, and PR signals to an inverse signal converter 61 via the switch 59. The inverse signal converter 61 has a function inverse with respect to the function of the signal converter 15 in the recording side of the apparatus. The inverse signal converter 61 combines the second reproduced Y, PB, and PR signals into a second composite NTSC signal. The inverse signal converter 61 outputs the second compos-

ite NTSC signal to a switch or selector 55. In addition, the TCI signal generator 53 outputs the recovered information signal to the switch 55. The switch 55 interposes the information signal in a time segment of the second composite NTSC signal which relates to the 19-th line of every frame. The switch 55 outputs the resultant second composite NTSC signal to a D/A converter 68. The resultant second composite NTSC signal is converted by the D/A converter 68 into a second analog NTSC signal "jj". The D/A converter 68 outputs the second analog NTSC signal "jj" to a transmission line (not shown).

Reproduction of an audio signal will now be described. FM audio signals of the right and left channels (the main and sub channels in the case of "bilingual") are reproduced from the magnetic tape TT by the audio heads 3A and 3B. The reproduced FM audio signals are fed to band pass filters 85 and 86 tuned to 1.7 MHz and 1.3 MHz respectively. The reproduced FM audio signals are separated from each other by the band pass filters 85 and 86. The reproduced FM audio signal of the right channel (the main channel in the case of "bilingual") is selected by the band pass filter 85 before being fed to an FM demodulator 87. The reproduced FM audio signal of the left channel (the sub channel in the case of "bilingual") is selected by the band pass filter 86 before being fed to an FM demodulator 88. The FM audio signals of the right and left channels are demodulated by the devices 87 and 88 into base-band reproduced audio signals 87a and 88a of the right and left channels which are fed to a switch or selector 89. The switch 89 receives the output signal 50a from the TCI discriminator 50 which contains the reproduced audio identification (discrimination) information. The switch 89 also receives audio control signal 89a which is generated by a suitable device (not shown) in response to operator's requirement. The switch 89 selects the reproduced audio signals 87a and 88a in response to the audio identification information 50a and the audio control signal 89a, and outputs the selected signals to transmission lines (not shown) as output audio signals "yy" and "zz".

In the case where the audio identification information 50a represents "bilingual", when the audio control signal 89a requires the main language, the switch 89 selects the main-channel audio signal 87a as the output audio signals "yy" and "zz". In the case where the audio identification information 50a represents "bilingual", when the audio control signal 89a requires the sub language, the switch 89 selects the sub-channel audio signal 88a as the output audio signals "yy" and "zz".

As shown in FIG. 20, the switch 89 includes a combination of a logic circuit 89A and switching sections 89B and 89C. The logic circuit 89A executes given logic operation between the audio identification information 50a and the audio control signal 89a. The switching section 89B selects one of the reproduced audio signals 87a and 88a as an output audio signal "yy" in response to an output signal of the logic circuit 89A. The switching section 89C selects one of the reproduced audio signals 87a and 88a as an output audio signal "zz" in response to an output signal of the logic circuit 89A.

As previously described, the audio identification information 50a represents the type of the audio signal (the stereophonic type, the monophonic type, or the bilingual type). Desired audio effects may be set for the stereophonic type, the monophonic type, and the bilingual type respectively. In this case, one of the desired audio effects which corresponds to the present audio-signal type is automatically selected and outputted in response to the audio identification information 50a.

With reference to FIG. 18, a VTR (video tape recorder) AA includes the signal recording and reproducing apparatus of the embodiment. The VTR AA is connected to a picture display apparatus BB such as a TV set which contains a data line decoder.

The picture display apparatus BB is designed so that it can handle a bilingual audio signal. The data line decoder extracts the audio identification information from an output HD signal of the VTR AA.

In the case where the picture display apparatus BB is preset by the operator to output the main language, when the audio identification information indicates "bilingual", the picture display apparatus BB automatically selects the main language from an output audio signal of the VTR AA in response to the audio identification information and then outputs the selected main language.

With reference to FIG. 19, a VTR (video tape recorder) AA includes the signal recording and reproducing apparatus of the embodiment. The VTR AA is connected to an AV (audio visual) amplifier CC which contains a data line decoder. The AV amplifier CC is designed so that it can provide a surround effect regarding a stereophonic audio signal. The data line decoder extracts the audio identification information from an output signal of the VTR AA. In the case where AV amplifier CC is preset by the operator to provide the surround effect, when the audio identification information indicates "stereophonic", the AV amplifier CC automatically implements the surround effect on the stereophonic audio signal in response to the audio identification information.

While the embodiment of this invention uses the dividers 201 and 480 to identify the types of the corrective signals in response to the time code signal, one of the corrective signals may be sequentially selected in response to the time code signal by other suitable arrangements. For example, a ROM storing the corrective signals may be used which is accessed in response to an address signal composed of the first word of the time code signal. In the case of two different corrective signals, it is sufficient to use only the lowest bit of the first word of the time code signal for sequential selection thereof.

While the TCI discriminator 50 and 51 processes the output signals of the correcting sections 46 and 47 in the embodiment of this invention, the TCI discriminator 50 and 51 may be modified to process the output signals of the A/D converters 44 and 45.

As previously described, the time code signal is reset to "0" at a recording start. The control signal 201a assumes "0" when the time code signal is "0". The gray scale signals for adjusting the direct-current levels and the amplitude levels between the even-line processing system and the odd-line processing system may be generated when the control signal 201a is "0". This design enables recording of the gray scale signals at a recording start.

The signal recording and reproducing apparatus of the embodiment may be modified to record and reproduce video information and audio information into and from a recording medium such as an optical disk, a floppy disk, or a semiconductor memory different from a magnetic tape.

The recording side or the reproducing side may be omitted from the signal recording and reproducing apparatus of the embodiment.

What is claimed is:

1. A video signal reproducing apparatus comprising:
means for reproducing a video signal from a recording medium, the video signal containing a time code signal

25

and a corrective signal, the time code signal being incremented every field or frame of the video signal, the corrective signal being sequentially selected from among predetermined R different corrective signals in response to a remainder of dividing a number represented by the time code signal by a predetermined natural number Q equal to or greater than 2, wherein R denotes a predetermined natural number equal to or smaller than the number Q;

means for extracting the time code signal from the reproduced video signal;

means for dividing the number represented by the time code signal by the number Q, and generating a signal representing a remainder of said dividing;

means for identifying the corrective signal in the reproduced video signal in response to the remainder-representing signal; and

means for correcting the reproduced video signal in response to a result of said identifying.

2. A video signal reproducing apparatus comprising:

means for reproducing a video signal from a recording medium, the video signal containing a time code signal and a corrective signal, the video signal further containing an information signal representing a presence and an absence of the corrective signal, the time code signal being incremented every field or frame of the video signal, the corrective signal being sequentially selected from among predetermined R different correc-

26

tive signals in response to a remainder of dividing a number represented by the time code signal by a predetermined natural number Q equal to or greater than 2, wherein R denotes a predetermined natural number equal to or smaller than the number Q;

means for extracting the time code signal from the reproduced video signal;

means for extracting the information signal from the reproduced video signal;

means for dividing the number represented by the time code signal by the number Q, and generating a signal representing a remainder of said dividing;

means for identifying the corrective signal in the reproduced video signal in response to the remainder-representing signal and the extracted information signal; and

means for correcting the reproduced video signal in response to a result of said identifying.

3. The apparatus of claim 2, further comprising means for reproducing an audio signal from the recording medium, means for extracting an audio identification signal from the reproduced video signal, the audio identification signal representing a type of the audio signal, means for outputting the reproduced audio signal in a changeable format, and means for setting said format in response to the audio identification signal.

* * * * *

EXHIBIT B

ADVISORY ACTION



RECEIVED
Advisory Action
JUL 09 2002
Technology Center 2000

Application No. 08/883,322	Applicant(s) SHIMIZU, RYOICHI	
Examiner Thai Tran	Art Unit 2615	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 March 2002 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ they raise the issue of new matter (see Note below);
(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attachment.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 1-14.

Claim(s) withdrawn from consideration: _____

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☐ Other: _____



RECEIVED
JUL 09 2002
Technology Center 2600

Application/Control Number: 08/883,322
Unit: 2615

Page 2

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed March 25, 2002 have been fully considered but they are not persuasive.

In re pages 1-4, applicant argues that Okauchi, like Suzuki, does not disclose means for recording a first time code stepped in a non-drop frame format and a second time code stepped in a drop frame format on the recording medium together with the selected recording frame rate.

In response, the examiner respectfully disagrees. It is noted that the capability of **simultaneously** recording a plurality of time codes together with the selected frame rate is not recited in the claims. The Specification is not the measure of invention. Therefore, limitations contained therein can not be read into the claims for the purpose of avoiding the prior art. In re Spork, 55 CCPA 743, 386 F.2d 924, 155 USPQ 687 (1968). As discussed in the Final Office Action mailed December 31, 2001, Okauchi discloses the claimed recording two types of time codes (non-drop frame mode, 10 dummy bits, and drop frame mode, 8 dummy bits) together with the selected frame rate (NTSC, 29.97 frame per second).

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Tran whose telephone number is (703) 305-4725. The examiner can normally be reached on Mon. to Friday, 8:00 AM to 5:30 PM.



RECEIVED
JUL 09 2002
Technology Center 2600


Application/Control Number: 08/883,322
Art Unit: 2615

Page 3

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

TTQ
April 4, 2002


THAI TRAN
PRIMARY EXAMINER



RECEIVED
JUL 09 2002
Technology Center 2600

**Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01**

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may **NOT** be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.